## AN2690 Application note

## 19 V - 75 W adapter with pre-regulator PFC using the L6563 and the L6566A

## Introduction

This application note describes the characteristics and the features of a 75 W reference board, wide-range input mains and power-factor corrected. Its electrical specification is tailored on a typical high-end portable computer power adapter. The peculiarities of this design are very low standby power consumption and excellent global efficiency.

Figure 1. L6566A and L6563-75W adapter demonstration board (EVL6566A75WADP)


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## 1 Main characteristics and circuit description

The main characteristics of the SMPS are listed below:

- Universal input mains range: $90 \div 264 \mathrm{Vac}_{\mathrm{ac}}$ - frequency $45 \div 65 \mathrm{~Hz}$
- Output voltage: 19 V at 4 A continuous operation
- Mains harmonics: according to EN61000-3-2 Class-D
- Standby mains consumption: 0.22 W at $230 \mathrm{~V}_{\mathrm{ac}}$
- Overall efficiency: better than $86 \%$ without synchronous rectification
- EMI: according to EN55022 - Class-B
- Safety: according to EN60950
- Low profile design: 25 mm maximum height
- PCB: single-side, $70 \mu \mathrm{~m}, \mathrm{CEM}-1,78 \times 174 \mathrm{~mm}$, mixed PTH/SMT

The circuit is composed of two stages: a front-end PFC using the L6563 and a flyback converter based on the L6566A. The flyback stage works as master and it is dedicated to control the circuit operation including the standby and protections. Additionally, it switches on and off the PFC stage by means of a dedicated pin ( $\mathrm{V}_{\mathrm{cc}}$ _PFC), thus helping to achieve an excellent efficiency even at light load, with low complexity.

## Power-factor corrector

The PFC stage is dedicated to the mains harmonic reduction within the limits of the relevant European or Japanese standards. Additionally it delivers a regulated DC bus used by the downstream converter.

The PFC controller is the L6563 (U1), working in transition mode. It integrates all functions needed to control the PFC and interface the master converter. Its power stage topology is a conventional boost converter, connected to the output of the mains rectifier bridge. It includes the coil L2, the diode D3, the capacitor C6, and the power MOSFET Q2.

The transition mode operation is achieved sensing the coil core demagnetization by the L2 secondary winding (pins 8-3). The latter is connected to the L6563 pin \#11 (ZCD) by R4. A negative-going edge on this pin triggers the MOSFET's turn-on while the turn-off is driven by the CS pin level.

Power-factor correction is achieved modulating the boost current with the input rectified voltage sensed by the divider R7, R12, R15, R18.

The divider R2, R6, R28, R8 and R9 is dedicated to sense the output voltage and feed the information to the Error Amplifier, while the divider R3, R5, R11, R10 and R19, directly connected to the output voltage, is dedicated to protect the circuit in case of voltage loop fail.

To maximize the overall efficiency the PFC makes use of the "Tracking Boost Option". With this function implemented the PFC DC output voltage changes proportionally to the mains voltage. The L6563 implements this function just by adding a resistor (R30) connected to the dedicated pin (TBO, \#6). Furthermore, the tracking boost option allows the use of a smaller (and cheaper) inductor. In this case a $400 \mu \mathrm{H}$ inductor has been used while, with a fixed output voltage PFC working at similar operating frequency, a $700 \mu \mathrm{H}$ inductor is needed.

## Flyback power stage

The downstream converter, acting as master stage, is implementing the L6566A (U6), a new dedicated current mode controller. The nominal switching frequency, 60 kHz , has been
chosen to obtain a compromise between the transformer size and the harmonics of the switching frequency, optimizing the input filter size and the total solution cost. The MOSFET is a 800 V rated, STP10NK80ZFP, housed in the TO-220FP package, needing just a small heat sink. The transformer is layer type, using a standard ferrite size EER35. The transformer, designed according to the EN60950, is manufactured by TDK. The flyback reflected voltage is $\sim 130 \mathrm{~V}$, providing enough room for the leakage inductance voltage spike with still margin for reliability of the MOSFET. The rectifier D8 and the Transil D4 clamp the peak of the leakage inductance voltage spike at MOSFET turn-off.

The output rectifiers are two dual center tap Schottky diodes (D7 and D5) in parallel. They have been selected according to the maximum reverse voltage, forward voltage drop and power dissipation. The snubber made up of R14, R66 and C8 damps the oscillation produced by the diode capacitance and the leakage inductance. A small LC filter has been added on the output, filtering the high frequency ripple.

D17, R75-R78, Q10 and Q15 implement an output voltage "fast discharge" circuit discharging quickly the output capacitors when the converter is turned off. It has been implemented to quickly decrease the residual output voltage after the converter is turned off at no load.

## Startup sequence

The circuit is designed so that at startup the flyback starts first, then it turns on the PFC stage controlling the L6563 via the $\mathrm{V}_{\text {cc_P }}$ PFC pin. Therefore, the flyback stage is designed to manage at startup the full output power over the entire input voltage range because it must guarantee the regulation of the output voltage even during a load transition when the load is increasing, but the PFC is still not yet delivering the nominal output voltage. Of course this condition can be maintained only for short time, typically tens of milliseconds, because the flyback is not designed to sustain this condition from a thermal point of view. The flyback controller L6566A pin \#1 (HV) is directly connected to the DC bulk voltage and at startup, an internal high voltage current source charges C32 and C33 until the device turn-on voltage threshold is reached, then the high voltage current source is automatically switched off. As the IC starts switching it is initially supplied by the $\mathrm{V}_{\mathrm{cc}}$ capacitor, the transformer auxiliary winding (pins 8-9) provides the voltage to power the IC. Afterwards, according to the load level, monitored by the COMP pin, the L6566A activates the L6563, powering it via the $\mathrm{V}_{\mathrm{cc}}$ PFC pin.

Because the L6566A integrated HV startup circuit is turned off, it is not dissipative during normal operation and contributes considerably in reducing power consumption when the power supply operates at light load. This reduction is significant in meeting worldwide standards currently required for standby power.

## Brownout protection

Brownout protection prevents the circuit from working with abnormal mains levels. It can be easily achieved using pin \#16 (AC_OK). Q3, C23, R62 and R64 implement a circuit sensing the rectified input voltage peak value and feed it into the pin \#16. An internal comparator then enables the IC operations if the mains level is correct, within the nominal limits. If the input voltage is below $90 \mathrm{Vac}_{\mathrm{ac}}$ the startup of the circuit is inhibited, while the turn-off voltage has been set at the voltage reached by the bulk capacitor after the hold-up time. The internal comparator has in fact a hysteresis allowing to set independently the L6566A turn-on and turn-off voltage. Sensing the input voltage before the input rectifier allows faster restart because there is no need to wait for the bulk capacitor discharge.

The L6563 has a similar protection on the RUN pin (\#10) but in this schematic it is not used because in this architecture it acts as slave, therefore the main controls are managed by the flyback stage.

## Output voltage feedback loop

The output regulation is done by means of two control loops, a voltage and a current one working alternatively. A dedicated control IC, the TSM1014 (U5), has been used. It integrates two operational amplifiers (used as error amplifiers) and a precise voltage reference. The output signal of the error amplifiers drives an optocoupler SFH617A-4 (U3) to get the required insulation of the secondary side and modulates the voltage on the COMP pin (\#9) of the L6566A.

## L6566A current mode control and voltage feed-forward function

R52 and R53 sense the Q5 MOSFET current of the flyback and the signal is fed into pin \#7 (CS), connected to the PWM comparator. This signal is thus compared with the COMP (pin \#9) signal, which is coming from the optocoupler.

The maximum power that the converter can deliver is set by a comparator limiting the peak of the primary current, comparing the CS and an internal threshold (VCSX). If the current signal exceeds the threshold, the comparator limits the MOSFET duty cycle, hence the output power is limited too.

Because the maximum transferable power depends on both the primary peak current and the input voltage, in order to keep almost constant the overload set point that would change according to flyback input voltage, the controller implements a voltage feed-forward function via a dedicated pin. Hence, VCSX is modulated by the voltage on pin \#15 (VFF) sensing the bulk voltage by a resistor divider. A higher voltage causes a smaller VCS,MAX so that the maximum power can be kept almost constant at any input voltage.

The resistor R60 connected between pin \#7 (CS) and pin \#12 (MODE/SC) provides the correct slope compensation to the current signal, required for the correct loop stability.

## L6566A short-circuit protection

In case of a short, an internal comparator senses the COMP pin after the soft-start time. In that condition the COMP pin goes high, activating an internal current source that restarts to charge the soft-start capacitor from the initial 2 V level. If the voltage on this pin reaches 5 V , the L6566A stops the operation and enters in "Hiccup mode". The device restarts with a startup sequence when the $\mathrm{V}_{c c}$ voltage drops below the $\mathrm{V}_{c c}$ restart level ( 5 V ). Because of the long time needed by the $\mathrm{V}_{\mathrm{cc}}$ capacitor to drop to 5 V , this results in an increase of the duration of the no-load operation, thus decreasing the power dissipation and the stress of power components. This sequence is repeated until the short is removed, subsequently the normal operation of the converter is automatically resumed.

Another comparator having its threshold at 1.5 V dedicated to protecting the circuit in case of transformer saturation or secondary diodes short is provided too. If the voltage on the CS pin (\#7) exceeds this threshold two consecutive times, the IC immediately shuts down and latches off. This is intended to prevent spurious activation of the protection in case of temporary disturbances, for example during the immunity tests. Even in this case the IC operation is resumed as soon as the $\mathrm{V}_{\mathrm{cc}}$ voltage drops below 5 V . In this way a hiccup mode operation is still obtained, avoiding consequent failures due to the power components overheating.

## Overvoltage protection

The pin \#11 (ZCD) is connected to the auxiliary winding by a resistor divider. It implements the OVP against feedback network failures. When the ZCD pin voltage exceeds 5 V the IC is shut down. This protection can be set as latched or auto-restart by the user with no additional components. On the board it is set as latched. Therefore the operations can be resumed after a mains recycling.

## Overtemperature protection

The thermistor R58, connected to the L6566A DIS pin (\#8), provides for a thermal protection of the flyback MOSFET (Q5). The L6563 PWM_LATCH pin (activated in case of PFC loop failures or PFC inductor saturation) is connected to L6566A DIS pin. Hence in case of PFC latching failures, the flyback converter activity is latched too. To maintain this state, an internal circuitry of the L6566A monitors the $\mathrm{V}_{\mathrm{cc}}$ and periodically reactivates the HV current source to supply the IC, while the PFC remains inactive after latching because it is no longer powered via the $\mathrm{V}_{\text {cc_ }}$ PFC pin that has been opened by the internal L6566A logic.

## Standby power saving and light-load frequency foldback function

The L6566A implements a current mode control, thus it monitors the output power by pin COMP, which level is proportional to the load. Thus, when the voltage on pin COMP falls below an internal threshold, the controller is disabled and its consumption reduced. Normal operation restarts as soon as the COMP voltage rises again. In this way a low consumption burst mode operation is obtained.

In this board, because the flyback stage acts as master, it has been electrically designed to operate over the entire mains voltage range. This solution allows turning off the PFC controller during no load operation, so saving power. As soon as the COMP level falls below the burst mode threshold, the L6566A stops supplying the PFC controller, disabling the $\mathrm{V}_{\text {cc_ }} \mathrm{PFC}$ pin. In this way the PFC consumption is reduced to almost zero and the converter's overall consumption is minimized.

The burst mode feature is dedicated to reduce the no-load consumption but another target of this application is achieving a high converter efficiency even at light load ( $0.5 \mathrm{~W}-3 \mathrm{~W}$ ), when normally it is quite low. To improve the efficiency at this load condition a reduction of the switching frequency is needed, in order to save AC and transition losses of the power section. A simple circuit having a frequency foldback, connected to the L6566A oscillator (pin \#13-OSC) is implemented on the board. This solution allows improving light-load efficiency requiring just three external components.

Figure 2. Electrical schematic


## 2 Test results

## Efficiency measurement

Figure 3 shows the overall efficiency vs. load, measured at different mains voltages. As shown the efficiency at nominal load ( 75 W ) is better than $86 \%$. This value is significantly high, especially if we compare this data with similar converters using two stages and the downstream converter implements a flyback.

Figure 3. EVL6566A-75WADP overall efficiency measurements vs. load


The diagram shows the efficiency is not monotonic because of the different contribution of the switching losses: in fact being the circuit operating at fixed frequency and discontinuous mode, the flyback MOSFET can turn on at any point between the peak and the valley of the ringing due to the resonance between the magnetizing inductance and the drain capacitance, depending by the input voltage and the output load. The phenomenon is visible comparing the drain waveforms in Figure 6 and Figure 7. Because of a different turn-on voltage provides different commutation losses, if we put in on a diagram the efficiency as a function of the output load and input voltage we'll find that the efficiency has not a flat trend.

## Harmonic content measurement

The board has been tested according to the European rule EN61000-3-2 Class-D and Japanese rule JEIDA-MITI Class-D, at both the nominal input voltage mains. As shown in Figure 4 and 5 the circuit is able to reduce the harmonics well below the limits of both regulations.

Figure 4. EVL6566A-75WADP compliance to EN61000-3-2 standard at $230 \mathrm{Vac}_{\mathrm{ac}}$ 50 Hz , full load


Figure 5. EVL6566A-75WADP compliance to JEIDA-MITI standard at100 $\mathrm{Vac}^{-}$ 50 Hz , full load


On the bottom of the diagrams the total harmonic distortion and power factor have been measured too. The values in all conditions give a clear idea of the correct function of the PFC even if it has implemented the tracking boost option.

## 3 Functional check

Figure 6 and 7 show some flyback waveforms during steady state operation. At nominal load conditions, the L6566A switching frequency has been set to 60 kHz in order to obtain good efficiency and limit the conducted EMI. The graphs show the L6563 TBO function, setting different PFC output voltage according to the mains input voltage.

Figure 6. EVL6566-75WADP flyback stage waveforms at $115 \mathrm{~V}-60 \mathrm{~Hz}$ - full load


CH 1 : Drain voltage
CH2: CS pin voltage
CH3: Gate voltage
CH4: PFC output voltage

Figure 7. EVL6566-75WADP flyback stage waveforms at $230 \mathrm{~V}-\mathbf{5 0 ~ H z}$ - full load

CH 1: Drain voltage
CH2: CS pin voltage
CH3: Gate voltage
CH4: PFC output voltage

## Standby and no-load operation

Figure 8 and 9 show some no-load waveforms. As shown, the L6566A works in burst mode. When the feedback voltage at pin COMP falls below 2.85 V (typical), the IC is disabled and its consumption is reduced. The chip is re-enabled as the voltage on pin COMP rises again over this threshold. Additionally, in order to get the best efficiency, during light-load operation the PFC stage is turned off. In fact when the voltage on pin COMP falls below the burst mode threshold, the L6566A pin \#6 ( $\mathrm{V}_{\mathrm{cc}}$ _PFC) supplying the PFC controller is opened. Thus the residual consumption of the PFC control circuitry is minimized to a negligible level. Whenever the IC is shut down, either latched or not, the $\mathrm{V}_{\text {cc_ }}$ PFC pin is open as well. To avoid undesired PFC turn-off during load transitions, $\mathrm{V}_{\text {cc_ }}$ PFC is opened 10 msec after the flyback stops switching.

Figure 8. EVL6566-75WADP no-load operation waveforms at $90 \mathrm{~V}-60 \mathrm{~Hz}$


CH : Drain voltage
CH : $\mathrm{V}_{\mathrm{cc}}$
CH3: COMP pin voltage

Figure 9. EVL6566-75WADP no-load operation waveforms at $265 \mathrm{~V}-50 \mathrm{~Hz}$

In Figure 10 and 11 the transitions from full load to no load and vice versa at maximum input voltage have been checked. The maximum input voltage has been chosen because it is the most critical input voltage for transition. In fact at no load the burst pulses have the lower repetition frequency and the $\mathrm{V}_{\mathrm{cc}}$ could drop, causing restart cycles of the controller. As shown in the graphs, both transitions are clean and there isn't any output voltage or $\mathrm{V}_{\mathrm{cc}}$ dip, or restarting attempt that could affect the proper power supply operation.

Figure 10. EVL6566-75WADP transition full load to no load at $265 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$

CH : Drain voltage
CH2: $\mathrm{V}_{\mathrm{cc}}$
CH3: Output voltage
CH4: Output current

Figure 11. EVL6566-75WADP transition no load to full load at $265 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$

Table 1 gives the power consumption from the mains during no-load operation. Thanks to the L6566A standby functionalities the input power is always below 280 mW .

Table 1. Input power at no load vs. mains voltage

| Vin [Vrms] | Input power [W] |
| :---: | :---: |
| 90 | 0.100 |
| 115 | 0.110 |
| 230 | 0.218 |
| 265 | 0.275 |

As referenced in Table 2, the most important international energy saving program regulations are given. This chipset is compliant to all regulations, mandatory or voluntary, applied currently or that will become effective in the near future.

Table 2. International energy saving programs regulations at no load

| Energy program | Effective date | Maximum admitted | Compliant |
| :---: | :---: | :---: | :---: |
| EU code of conduct | Jan 2007 | 300 mW | Yes |
| Energy star int. | Jan 2008 | 750 mW | Yes |
| California energy <br> commission | Jul 2008 | 500 mW | Yes |
| Group for energy- <br> efficient appliances | Jan 2007 | 300 mW | Yes |

The new regulations and voluntary agreements that are coming require that power supplies and adapters have high efficiency at not only nominal or maximum load but also at light load. This last condition is frequently a difficult task to achieve, increasing the complexity of the control part. As previously explained, thanks to the oscillator structure of the L6566A, just by adding few external components, a frequency foldback circuit can be implemented. Thus, reducing switching losses improves the power supply efficiency when it is delivering an output power in the range of 0,5 to 3 W .

The L6566A switching frequency is set by the current flowing in a resistor connected between the OSC pin and ground (R42). During light-load operation Q5 (Figure 12) injects into R42 a current inversely proportional to the COMP voltage. The voltage on pin OSC is constant ( 1 V ) so, increasing Q5 current allows decreasing the current supplied by the pin and, as a consequence, the oscillator frequency. In this way the converter switching losses, prevailing at light load, are reduced.

Figure 12. Frequency foldback circuit


## Equation 1

$$
\mathrm{f}_{\mathrm{osc}} \approx \frac{2 \cdot 10^{3}}{\mathrm{R} 42}
$$

## Equation 2

$$
f_{\text {fold }- \text { back }} \approx 2 \cdot 10^{3}\left(\frac{1}{R 42}-I_{Q 5}\right)
$$

Figure 13 and 14 show the input power consumption and the efficiency of the board working at light-load conditions, for example when a power supply is powering a laptop during power-saving operation.

Figure 13. EVL6566A-75WADP o/p power vs. Figure 14. EVL6566A-75WADP light-load input power at light load efficiency


As shown, the input power consumption is always very low and the efficiency remains significantly high even at output power levels where normally the power supply's efficiency drops.

## Overcurrent and short-circuit protection

In this evaluation board the overcurrent is managed by a TSM1014 (U5), a CC/CV controller. Inside the IC there are a voltage reference and two Or-ed operational amplifiers, one dedicated to act as the error amplifier of the voltage loop and the second is dedicated to act as the error amplifier of the current loop. During normal operation the voltage feedback loop is working while, in case the output current exceeds the programmed value, the current loop error amplifier takes over, thus keeping constant the output current.

In case of a dead-short, the current cannot be limited effectively by U5 because the output voltage drops so it is unpowered, therefore the primary controller must manage the failure condition.

L6566A detects a short-circuit monitoring the control pins. When the output voltage drops and consequently pin COMP saturates high, the soft-start capacitor is charged by an internal current source. When the Vss voltage reaches an internal disable threshold, the controller stops switching and remains in the off-state until the voltage on the $\mathrm{V}_{\mathrm{cc}}$ pin decreases below the $\mathrm{V}_{\mathrm{cc}}$ restart threshold ( 5 V ). Then, the HV startup turns on and charges the $\mathrm{V}_{\mathrm{cc}}$ capacitor. As soon as the turn-on threshold is reached, the circuit restarts. If the short is still there, the circuit just attempts to restart but it stops in few milliseconds. Restart attempts are repeated indefinitely, until the short is removed. This provides a very low frequency hiccup working mode (for this board 0.5 Hz ), limiting the current flowing at secondary side (less than 1Arms) preventing the power supply from overheating, which could destroy it.

Figure 15 shows the circuit behavior in case of a short-circuit.

Figure 15. Short circuit at full load and $230 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$


CH1: Gate voltage
CH2: V
CH3: SS pin voltage
CH 4 : Output current

Figure 16. Short circuit detail at no load $230 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$


CH 1: Drain voltage
CH2: COMP pin voltage
CH3: SS pin voltage
CH4: Output current

Thanks to the functionalities of the L6566A and the TSM1014, the protection levels and the timing of the fault protection sequences described in Figure 15 and 16 do not change significantly over the entire input voltage range of the board.

In these figures we can note that during the SS voltage ramping up, the transferred power is limited, and in Figure 15 the mean value of the output current is measured and it is well below the nominal level. Additionally, in Figure 16 we can see that when the soft-start pin voltage reaches the IC disable threshold, the L6566A stops switching. This feature allows implementing a delayed OCP protection useful in several applications having to manage load with pulsed absorption (like printers or hard disk motors at spin-up) by just selecting a proper value of the soft-start capacitor.

## Overvoltage and open-loop protection

The EVL6566-75WADP board implements two different open-loop protections, one for each stage.

The PFC controller L6563 is equipped with an OVP monitoring the current flowing through the compensation network and entering in the error amplifier (pin COMP, \#2). When this current reaches about $18 \mu \mathrm{~A}$ the output voltage of the multiplier is forced to decrease, thus reducing the energy drawn from the mains. If the current exceeds $20 \mu \mathrm{~A}$, the OVP is triggered (Dynamic OVP), and the external power transistor is switched off until the current falls approximately below $5 \mu \mathrm{~A}$. However, if the overvoltage persists (e.g. in case the load is completely disconnected), the error amplifier eventually saturates low, triggering an internal comparator (Static OVP) that keeps the external power switch turned off until the output voltage comes back close to the regulated value.

The OVP function described above is able to handle "normal" overvoltage conditions, i.e. those resulting from an abrupt load/line change or occurring at startup. It cannot handle the overvoltage generated, for instance, when the upper resistor of the output divider fails open. The voltage loop can no longer read the information on the output voltage and forces the PFC pre-regulator to work at maximum ON-time, causing the output voltage to rise with no control.

A pin of the L6563 (PFC_OK, \#7) has been dedicated to provide additional monitoring of the output voltage with a separate resistor divider (R3, R5, R11 high, R10 and R19 low). This divider is selected so that the voltage at the pin reaches 2.5 V if the output voltage exceeds a preset value, usually larger than the maximum Vo that can be expected, also including overshoots due to worst-case load/line transients.

When this function is triggered, the gate drive activity is immediately stopped, the device is shut down, its quiescent consumption is reduced below $250 \mu \mathrm{~A}$ and the condition is latched as long as the supply voltage of the IC is above the UVLO threshold. At the same time the pin PWM_LATCH (pin \#8) is asserted high. PWM_LATCH is an open source output able to deliver 3.7 V min. with 0.5 mA load, intended for tripping a latched shutdown function of the PWM controller IC in the cascaded DC-DC converter, so that the entire unit is latched off. In the EVL6566-75WADP the PWM_LATCH is connected to the DIS pin of theL6566A, thus disabling also the flyback stage as described. To restart the system it is necessary to recycle the input power, so that the $\mathrm{V}_{\mathrm{cc}}$ voltages of both the L6563 and the L6566A fall below their respective UVLO thresholds. The PFC_OK pin doubles its function as a not-latched IC disable. A voltage below 0.2 V shuts down the $I C$, reducing its consumption below 1 mA . In this case both PWM_STOP and PWM_LATCH keep their high impedance status. To restart the IC simply let the voltage at the pin rise above 0.26 V .

Note that this function offers a complete protection against not only feedback loop failures or erroneous settings, but also against a failure of the protection itself. Either resistor of the PFC_OK divider failing short or open or the PFC_OK (\#7) pin floating, results in shutting down the L6563 and stopping the controller operation of the flyback stage.

Figure 17. EVL6566-75WADP PFC open loop at $115 \mathrm{Vac}_{\mathrm{ac}}-60 \mathrm{~Hz}$ - full load


The event of an open loop is shown in Figure 17. We can notice the protection intervention stopping the operation of the L6563 and the activation of the PWM_LATCH pin that is connected to the L6566A pin \#7 (DIS). This function of the L6566A is a latched device shutdown. Internally the pin connects a comparator that, when the voltage on the pin exceeds 4.5 V , shuts down the IC and brings its consumption to a value barely higher than before startup. The internal L6566A logic also opens the pin $\mathrm{V}_{\text {cc_P }}$ PFC, therefore the L6563 remain inactive after latching because it is no longer powered.

This state is latched and it is necessary to recycle the input power to restart the IC. The latch is removed as the voltage on the $\mathrm{V}_{\mathrm{cc}}$ pin falls below the UVLO threshold.
The flyback stage is protected too against open loop conditions that lead to losing control of the output voltage.

The L6566A OVP function monitors the voltage on the ZCD pin (\#11) during the MOSFET's OFF-time, during which the voltage generated by the auxiliary winding tracks the converter's output voltage. If the voltage on the pin exceeds an internal 5 V reference, an overvoltage condition is assumed and the device is shut down. An internal current generator is activated that sources 1 mA out of the VFF pin (\#15). If the VFF voltage is allowed to reach 2 VBE over 5 V , the L6566A is latched off (Figure 18). As soon as the IC is latched, $\mathrm{V}_{\mathrm{CC}}$ starts decreasing until it reaches a value 0.5 V below the turn-on threshold. Then the HV startup circuit turns on and begins to operate periodically in order to keep $\mathrm{V}_{\mathrm{cc}}$ between $\mathrm{V}_{\mathrm{cc}} \mathrm{ON}$ and $\mathrm{V}_{\mathrm{cc}} \mathrm{ON}-0.5 \mathrm{~V}$ (Figure 19) maintaining the IC latched.

Figure 18. Flyback open loop at $230 \mathrm{Vac}_{\mathrm{ac}}-50 \mathrm{~Hz}$ Figure 19. Flyback open loop at $230 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$

- half load


CH1: $\mathrm{V}_{\mathrm{FF}}$ voltage
CH2: $\mathrm{V}_{\mathrm{cc}}$
CH3: ZCD voltage
CH4: Output voltage - half load


CH1: $\mathrm{V}_{\mathrm{FF}}$ voltage
CH2: $\mathrm{V}_{\text {cc }}$
CH3: ZCD voltage
CH4: Output voltage

If R37 is shorted, the impedance externally connected to pin \#15 ( $\mathrm{V}_{\mathrm{FF}}$ ) is lower and the voltage in case of OVP cannot reach the 5+2VBE threshold so the L6566A restarts after the $\mathrm{V}_{\mathrm{cc}}$ has dropped below 5 V . In case of L6566A OVP intervention, the L6563 operation is stopped too because the L6566A stops the PFC via the $\mathrm{V}_{\text {cc- }}$ PFC pin.
In Figure 18 it is also possible to note that the signal at ZCD pin has on the leading edge the typical spike at MOSFET turn-off due to the transformer leakage inductance. Thanks to the digital circuitry integrated in the L6566A it doesn't influence the correct behavior of the IC. In fact an internal $2 \mu \mathrm{~s}$ (typ.) blanking time at MOSFET turn-off delays the sampling ( $0.5 \mu \mathrm{~s}$ ) of the signal that in that region is clean and therefore perfectly linked to the output voltage.
Additionally, to improve the immunity against temporary disturbances (needed for example in case of immunity tests), an internal logic activates the protection after the OVP has been detected for 4 consecutive switching cycles.

Figure 20. Flyback open loop - restart option $230 \mathrm{Vac}_{\mathrm{ac}} \mathbf{5 0 \mathrm { Hz } \text { -half load }}$


Table 3 gives the output voltage at OVP intervention. The measures therefore demonstrate that, as previously explained, the L6566A sensing technique provides a very stable OVP intervention threshold over the entire mains voltage and load ranges.

Table 3. Output voltage at OVP intervention vs. input voltage and output power

| Input voltage | Output power | Output voltage at OVP intervention |
| :---: | :---: | :---: |
| 115 V | 75 W | 20.21 V |
| 115 V | 35 W | 20.19 V |
| 115 V | 0 W | 20.21 V |
| 230 V | 75 W | 20.22 V |
| 230 V | 35 W | 20.20 V |
| 230 V | 0 W | 20.22 V |

## 4 Thermal map

In order to check the design reliability, a thermal mapping by means of an IR camera was done. Figure 21 and 22 show the thermal measures of the board, component side, at nominal input voltage. Some pointers visible on the pictures have been placed across key components or components showing high temperature. The ambient temperature during both measurements was $27^{\circ} \mathrm{C}$. All other components of the board are working within the temperature limits, assuring a reliable long-term operation of the power supply.

Figure 21. Thermal map at $115 \mathrm{~V}_{\mathrm{ac}}-60 \mathrm{~Hz}$ - full load


Figure 22. Thermal map at $230 \mathrm{~V}_{\mathrm{ac}}-50 \mathrm{~Hz}$ - full load


Table 4. Thermal maps reference points

| Point | Reference | Description |
| :---: | :---: | :---: |
| A | D2 | Bridge rectifier |
| B | Q2 | PFC switch |
| C | R1 | NTC resistor |
| D | D4 | Flyback transformer clamping transil |
| E | Q5 | Flyback switch |
| F | T1 | Flyback power transformer |
| G | D5 | Output diodes |
| H | L1 | Input common mode filtering inductor |

## 5 Conducted emission pre-compliance test

Figure 23 and 24 show the peak measurement of the conducted noise at full load and nominal mains voltages. The limits shown on the diagrams are the EN55022 Class-B ones, which is the most popular rule (or standard) for domestic equipment and it has more severe limits compared to the Class-A, dedicated to IT equipment. As shown in the diagrams, under all test conditions the measures are within the limits.

Figure 23. CE peak measure at $115 \mathrm{~V}_{\mathrm{ac}}$ and full load


Figure 24. $C E$ peak measure at $230 \mathrm{~V}_{\mathrm{ac}}$ and full load


## 6 Bill of material (BOM)

Table 5. EVL6566A-75WADP evaluation board: bill of material

| Des. | Part type/part value | Description | Supplier |
| :---: | :---: | :---: | :---: |
| C1 | 2N2 | Y1 - safety cap. - DE1E3KX222M | MURATA |
| C2 | 2N2 | Y1 - safety cap. - DE1E3KX222M | MURATA |
| C3 | 470N | X2 - flm cap - R46-I 3470--M1- | ARCOTRONICS |
| C4 | 470N | X2 - flm cap - R46-I 3470--M1- | ARCOTRONICS |
| C5 | 470N-400 V | 400 V - flm cap - B32653A4474 | EPCOS |
| C6 | $100 \mu \mathrm{~F}-450 \mathrm{~V}$ | 450 V - Aluminum ELCAP - LLS series - $85{ }^{\circ} \mathrm{C}$ | NIPPONCHEMICON |
| C7 | 2N2 | Y1 - safety cap. - DE1E3KX222M | MURATA |
| C8 | 1N0 | 200 V CERCAP - general purpose | AVX |
| C9 | 100 N | 50 V CERCAP - general purpose | AVX |
| C12 | $1000 \mu-25 \mathrm{~V}$ | 25 V - Aluminum ELCAP - ZL series - $105{ }^{\circ} \mathrm{C}$ | RUBYCON |
| C13 | 100 $\mu$ - 25 V | 25 V - Aluminum ELCAP - YXF series - $105{ }^{\circ} \mathrm{C}$ | RUBYCON |
| C14 | 220 N | 50 V CERCAP - general purpose | AVX |
| C15 | $1 \mu$ | 25 V CERCAP - general purpose | AVX |
| C16 | $1000 \mu-25 \mathrm{~V}$ | 25 V - Aluminum ELCAP - ZL series - $105^{\circ} \mathrm{C}$ | RUBYCON |
| C17 | 100 N | 50 V CERCAP - general purpose | AVX |
| C19 | 2N2 | 50 V CERCAP - general purpose | AVX |
| C21 | 470N | 25 V CERCAP - general purpose | AVX |
| C23 | 100 N | 50 V CERCAP - general purpose | AVX |
| C24 | 2N2 | Y1 - SAFETY CAP. - DE1E3KX222M | MURATA |
| C25 | 220p | 50 V CERCAP - general purpose | AVX |
| C26 | 22N | 50 V CERCAP - general purpose | AVX |
| C30 | 2N2 | 50 V CERCAP - general purpose | AVX |
| C32 | 100 N | 50 V CERCAP - general purpose | AVX |
| C33 | $47 \mu \mathrm{~F}-50 \mathrm{~V}$ | 50 V - Aluminum ELCAP - YXF SERIES - $105^{\circ} \mathrm{C}$ | RUBYCON |
| C34 | 47N | 50 V CERCAP - general purpose | AVX |
| C35 | 220 N | 50 V CERCAP - general purpose | AVX |
| C36 | 100N | 50 V CERCAP - general purpose | AVX |
| C38 | 220p | 50 V CERCAP - general purpose | AVX |
| C39 | 100 N | 50 V CERCAP - general purpose | AVX |
| C40 | 10N | 50 V CERCAP - general purpose | AVX |
| C41 | 10N | 50 V CERCAP - general purpose | AVX |

Table 5. EVL6566A-75WADP evaluation board: bill of material (continued)

| Des. | Part type/part value | Description | Supplier |
| :---: | :---: | :---: | :---: |
| C43 | 2N2 | 50 V CERCAP - general purpose | AVX |
| C44 | 1 N | 50 V CERCAP - general purpose | AVX |
| D1 | 1N4005 | Rectifier - general purpose | VISHAY |
| D2 | GBU4J | Single-phase bridge rectifier | VISHAY |
| D3 | STTH2L06 | Ultrafast high voltage rectifier | STMicroelectronics |
| D4 | 1.5KE250A | TRANSIL | STMicroelectronics |
| D5 | STPS20H100CFP | High-voltage power Schottky rectifier | STMicroelectronics |
| D7 | STPS20H100CFP | High-voltage power Schottky rectifier | STMicroelectronics |
| D8 | STTH108A | High-voltage ultrafast rectifier | STMicroelectronics |
| D11 | STTH102A | Fast-switching diode | STMicroelectronics |
| D12 | LL4148 | Fast-switching diode | VISHAY |
| D16 | LL4148 | Fast-switching diode | VISHAY |
| D17 | BZV55-B18 | Zener diode | PHILIPS |
| F1 | FUSE 4 A | Fuse T4A - time delay | WICHMANN |
| HS1 | HEAT-SINK |  |  |
| HS2 | HEAT-SINK |  |  |
| HS3 | HEAT-SINK |  |  |
| J1 | MKDS 1,5/ 3-5,08 | PCB term. block, screw conn., PITCH 5MM - 3 W. | PHOENIX CONTACT |
| J2 | MKDS 1,5/ 2-5,08 | PCB term. block, screw conn., pitch 5MM - 2 W. | PHOENIX CONTACT |
| L1 | HF2422-203Y1R0-T01 | Input EMI filter | TDK |
| L2 | SRW25CQ-T05V102 | PFC inductor | TDK |
| L3 | TSL0706-1R5-4R3 | 1u5-Radial inductor | TDK |
| Q2 | STP9NK50ZFP | N-channel power MOSFET | STMicroelectronics |
| Q3 | BC847C | NPN small signal BJT | ZETEX |
| Q5 | STP10NK80ZFP | N-channel power MOSFET | STMicroelectronics |
| Q9 | BC857C | PNP small signal BJT | ZETEX |
| Q10 | BC847C | NPN small signal BJT | ZETEX |
| Q11 | BC847C | NPN small signal BJT | ZETEX |
| R1 | NTC 10R-S236 | NTC RESISTOR P/N B57236S0100M000 | EPCOS |
| R2 | $680 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R3 | 2M2 | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R4 | $68 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R5 | 2M2 | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |

Table 5. EVL6566A-75WADP evaluation board: bill of material (continued)

| Des. | Part type/part value | Description | Supplier |
| :---: | :---: | :---: | :---: |
| R6 | $680 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R7 | 3M3 | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R8 | $75 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R9 | $75 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R10 | $33 \mathrm{k} \Omega$ | SFR25 axial stand. film res - $0.4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R11 | 2M2 | SFR25 axial stand. film res - $0.4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R12 | 3M3 | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R14 | 3R9 | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R15 | $100 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R17 | $62 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R18 | $51 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R19 | 3K0 | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R22 | R015 | SMD film res 1 W - 2512 MSR1 | MEGGIT |
| R23 | $27 \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R24 | $100 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R25 | $470 \Omega$ | SFR25 axial stand. film res -0.4 W-5\%-250 ppm/ ${ }^{\circ} \mathrm{C}$ | VISHAY |
| R26 | 0R0 | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R27 | 0R33 | SFR25 axial stand. film res - $0.4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R28 | $680 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R30 | $22 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R31 | $39 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R32 | $15 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R33 | 0R0 | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R34 | $390 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R35 | 2R7 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R36 | 1 K 8 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R37 | $10 \mathrm{k} \Omega$ | SFR25 axial stand. film res - $0.4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R39 | $56 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R42 | $33 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R43 | 4R7 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R45 | 2K2 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R46 | $15 \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R47 | $100 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R48 | 4K7 | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R49 | 24K | SMD standard film res -1/8 W-1\%-100 ppm/ ${ }^{\circ} \mathrm{C}$ | VISHAY |

Table 5. EVL6566A-75WADP evaluation board: bill of material (continued)

| Des. | Part type/part value | Description | Supplier |
| :---: | :---: | :---: | :---: |
| R50 | 1K0 | SFR25 axial stand. film res - $0.4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R51 | 1K0 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R52 | OR56 | SFR25 axial stand. film res - $0.4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R53 | OR56 | SFR25 axial stand. film res -0.4 W-5\%-250 ppm/ ${ }^{\circ} \mathrm{C}$ | VISHAY |
| R54 | $47 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R55 | 22R | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R57 | 100R | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R58 | M57703 | THERMISTOR - B57703M103G | EPCOS |
| R59 | $12 \mathrm{k} \Omega$ | SFR25 axial stand. film res -0.4 W-1\%-100 ppm/ ${ }^{\circ} \mathrm{C}$ | VISHAY |
| R60 | 6 K 8 | SFR25 axial stand. film res - $0.4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R62 | $100 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R63 | $100 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R64 | $150 \mathrm{k} \Omega$ | SMD Standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R65 | $22 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R66 | 3R9 | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R67 | $12 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R68 | $220 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R69 | 1 KO | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R70 | $18 \mathrm{k} \Omega$ | SMD standard film res - $1 / 8 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R72 | 0R0 | SMD standard film res - $1 / 4 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R74 | $47 \mathrm{k} \Omega$ | SMD standard film res - $1 / 4 \mathrm{~W}-1 \%-100 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R75 | 1K8 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R76 | 4K7 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| R77 | $100 \mathrm{k} \Omega$ | SMD standard film res -1/8 W-5\%-250 ppm/ ${ }^{\circ} \mathrm{C}$ | VISHAY |
| R78 | 2K2 | SMD standard film res - $1 / 8 \mathrm{~W}-5 \%-250 \mathrm{ppm} /{ }^{\circ} \mathrm{C}$ | VISHAY |
| T1 | SRW32EC-T01H114 | Power transformer | TDK |
| U1 | L6563 | Transition-mode PFC controller | STMicroelectronics |
| U3 | SFH617A-4 | Optocoupler | INFINEON |
| U5 | TSM1014AIST | Low-consumption CC/CV controller | STMicroelectronics |
| U6 | L6566A | Multimode PWM controller | STMicroelectronics |

## $7 \quad$ PFC coil specification

## General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Coil former: vertical type, $5+3$ pins
- Max. temp. rise: $45^{\circ} \mathrm{C}$
- Max. operating ambient temp.: $60^{\circ} \mathrm{C}$
- Mains insulation: n.a.
- UT finishing: varnished


## Electrical characteristics

- Converter topology: boost, transition mode
- Core type: CQ25-PC47
- Min. operating frequency: 20 kHz
- Typical operating freq: 80 kHz
- Primary inductance: $400 \mu \mathrm{H} \pm 10 \%$ at $1 \mathrm{kHz}-0.25 \mathrm{~V}$ (see Note: 1)
- Peak primary current: 3.5 Apk
- RMS primary current: 1.2 Arms

Note: 1 Measured between pins \#5 and \#6

## Electrical diagram and winding characteristics

Figure 25. PFC coil electrical diagram


Table 6. PFC coil winding characterisctics

| PIns | Winding | RMS current | Number of <br> turns | Wire type |
| :---: | :---: | :---: | :---: | :---: |
| $8-3$ | AUX ${ }^{(1)}$ | $0.05 \mathrm{~A}_{\text {RMS }}$ | 5 spaced | $\phi 0.28 \mathrm{~mm}$ |
| $5-6$ | Primary ${ }^{(2)}$ | $1.2 \mathrm{~A}_{\text {RMS }}$ | 50 | Multistranded $\# 10 \mathrm{x}$ <br> $\phi 0.20 \mathrm{~mm}$ |

1. Aux. winding is wound on coil former before primary winding. To be insulated with a layer of polyester tape
2. Primary winding external insulation: 2 layers of polyester tape

## Mechanical aspect and pin numbering

- Maximum height from PCB: 20 mm
- COIL former type: vertical, 5+3 pins
- Pins \#1, 2, 4, 7 are removed
- External copper shield: not insulated, wound around the ferrite core and including the coil former. Height is 7 mm . Connected to pin \#3 by a solid wire.

Figure 26. PFC coil mechanical aspect

1. External COPPER sheet (0.025x7 mm)
2. Mylar tape - 1 turn


- $A: 27.0$ max mm
- $\quad \mathrm{B} 1: 3.0 \pm 0.3 \mathrm{~mm}$
- B2: $5.0 \pm 0.3 \mathrm{~mm}$
- $\mathrm{C}: 3.3 \pm 0.3 \mathrm{~mm}$
- D: 19.0 max mm
- E: $21.0 \pm 0.5 \mathrm{~mm}$
- $F: 23.7 \pm 0.5 \mathrm{~mm}$


## 8 Transformer specification

## General description and characteristics

- Application type: consumer, home appliance
- Transformer type: open
- Winding type: ayer
- COIL former: horizontal type, 9+9 pins
- Max. temperature rise: $45^{\circ} \mathrm{C}$
- Max. operating ambient temp.: $60^{\circ} \mathrm{C}$
- Mains insulation: acc. with EN60950
- Unit finishing: varnishing


## Electrical characteristics

- Converter topology: flyback, CCM/DCM mode
- Core type: EER34 - PC47
- Min. operating frequency: -
- Typical operating freq: 60 kHz
- Primary inductance: $550 \mu \mathrm{H} \pm 10 \%$ at $1 \mathrm{kHz}-0.25 \mathrm{~V}$ (see Note: 1 )
- Leakage inductance: $17 \mu \mathrm{H} \max$ at $100 \mathrm{kHz}-0.25 \mathrm{~V}$ (see Note: 2)
- Max. peak primary current: 2.65 Apk
- RMS primary current: 0.78 ARMS

Note: 1 Measured between pins $(2,3)-(5,6)$
2 Measured between pins $(2,3)-(5,6)$ with all secondary windings shorted

## Electrical diagram and winding characteristics

Figure 27. Transformer electrical diagram


Table 7. Transformer winding characterisctics

| Pins | Winding | O/P RMS <br> current | Number of <br> turns | Number of <br> layers | Wire type |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 5-6 | AUX | 0.05 A $_{\text {RMS }}$ | 7 spaced | 1 | G2 $-\phi 0.23 \mathrm{~mm}$ |
| 3-1 | Primary - A | $0.39 \mathrm{~A}_{\text {RMS }}$ | 60 | 2 | G2 $-2 \times \phi 0.23 \mathrm{~mm}$ |
| $8-10$ | 19 V | $5.2 \mathrm{~A}_{\text {RMS }}$ | 8 | 1 | Multistrand G2-4× 00.64 mm |
| $4-2$ | Primary - B | $0.39 \mathrm{~A}_{\text {RMS }}$ | 60 | 2 | G2- $2 \times \phi 0.23 \mathrm{~mm}$ |

Figure 28. Transformer winding diagram


Note: $\quad$ Primaries $A$ and $B$ are in parallel

## Mechanical aspect and pin numbering

- Maximum height from PCB: 30 mm
- Coil former type: horizontal, 9+9 pins (pins 2 removed)
- Pin distance: 4 mm
- Row distance: 35 mm
- External copper shield: not insulated, wound around the ferrite core and including the coil former. Height is 12 mm .

Figure 29. Transformer mechanical aspect


- A: 38.0 max mm
- B: $4.0 \pm 0.3 \mathrm{~mm}$
- C: $3.5 \pm 0.5 \mathrm{~mm}$
- D: 26.5 max mm
- E: 40.0 max mm
- $F: 35.0 \pm 0.5 \mathrm{~mm}$


## 9 Revision history

Table 8. Document revision history

| Date | Revision | Changes |
| :---: | :---: | :--- |
| 10-Jun-2008 | 1 | Initial release |

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