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World's Leading Company in Mixed Signal Technologies

To Our Customers

CEL continues to offer industry leading semiconductor products from Japan. We are pleased to add new communication products from THine Electronics to our product portfolio.

THC63LVD824A

Single(112MHz)/Dual(170MHz) Link LVDS Receiver for XGA/SXGA/SXGA+/UXGA

General Description

The THC63LVD824A receiver is designed to support Single Link transmission between Host and Flat Panel Display up to SXGA resolutions and Dual Link transmission between Host and Flat Panel Display up to UXGA resolutions. The THC63LVD824A converts the LVDS data streams back into 48bits of CMOS/TTL data with falling edge or rising edge clock for convenient with a variety of LCD panel controllers.

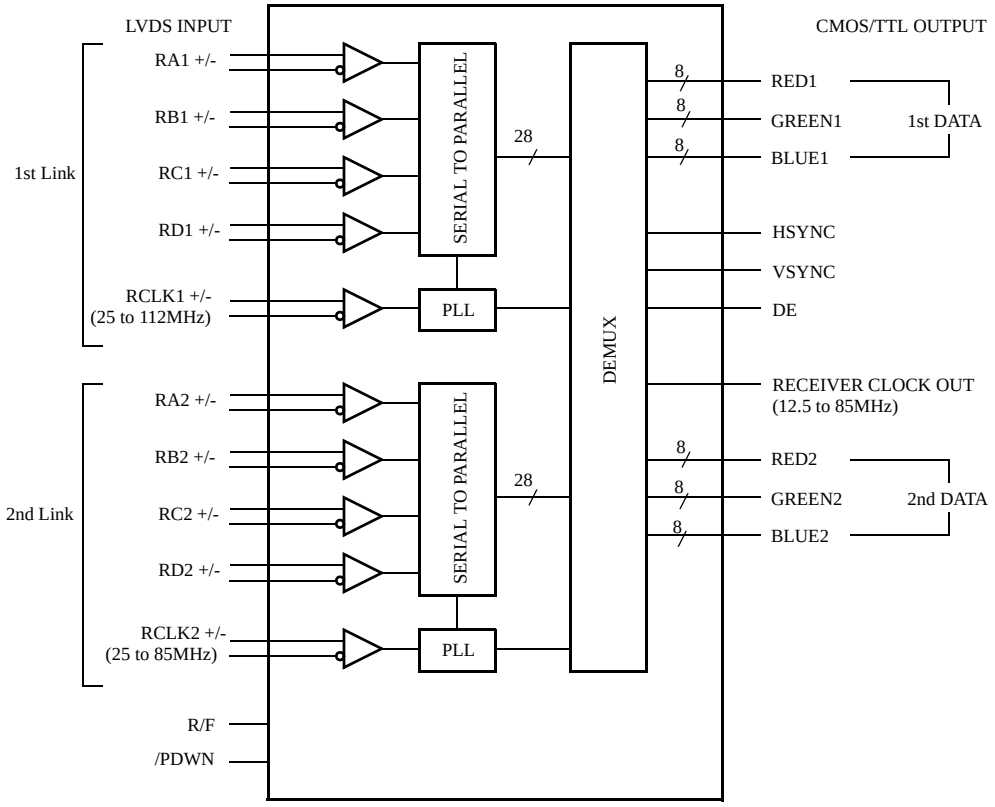
In Single Link, data transmit clock frequency of 112MHz, 48bits of RGB data are transmitted at an effective rate of 784Mbps per LVDS channel. Using a 112MHz clock, the data throughput is 392Mbytes per second.

In Dual Link, data transmit clock frequency of 85MHz, 48bits of RGB data are transmitted at an effective rate of 595Mbps per LVDS channel. Using a 85MHz clock, the data throughput is 595Mbytes per second.

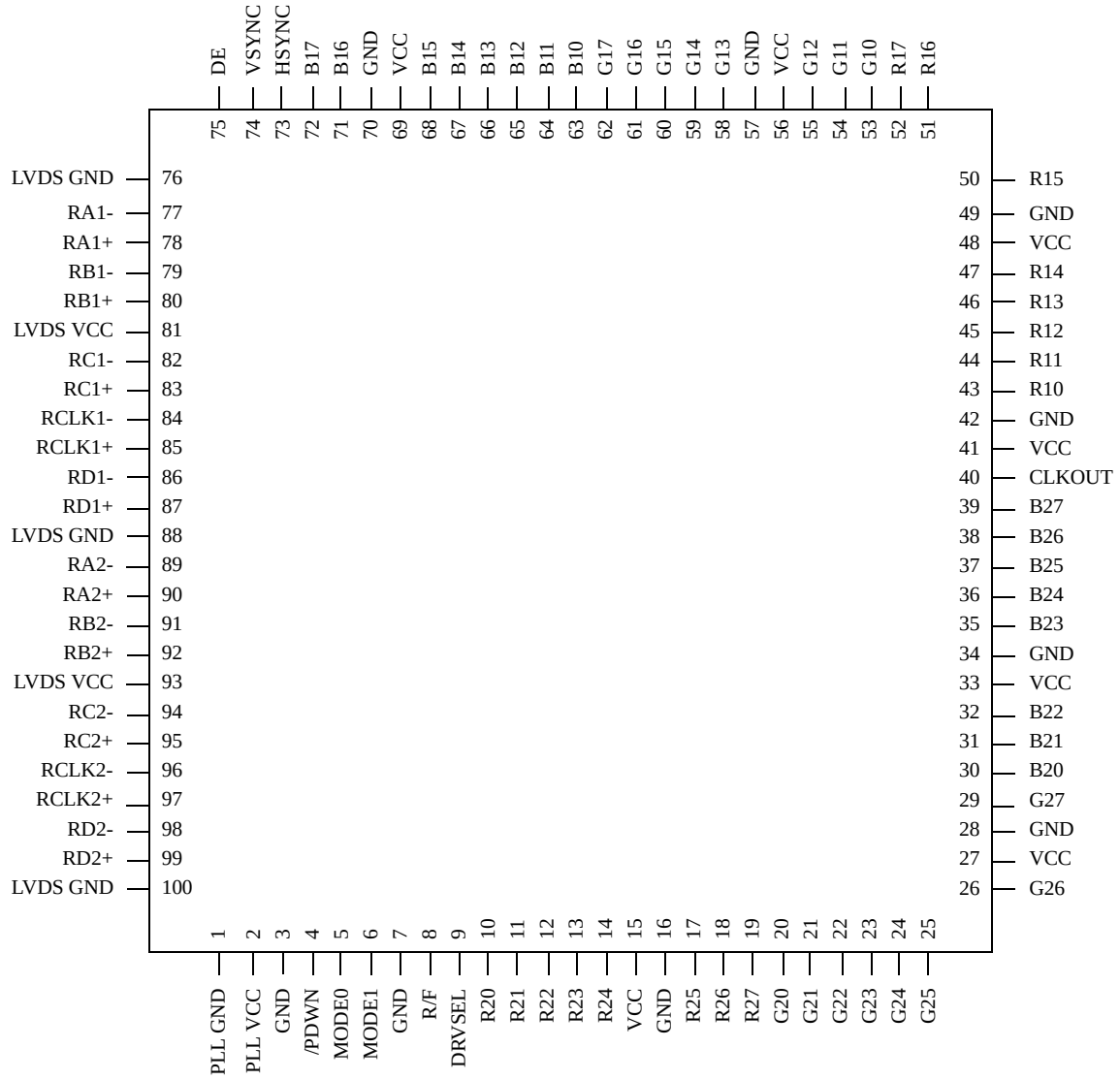
Features

- Wide dot clock range: 25-170MHz suited for VGA, SVGA, XGA, SXGA, SXGA+ and UXGA
- PLL requires No external components
- Supports Single Link up to 112MHz dot clock for SXGA
- Supports Dual Link up to 170MHz dot clock for UXGA
- 50% output clock duty cycle
- TTL clock edge programmable
- TTL output driverbility selectable for lower EMI
- Power down mode
- Low power single 3.3V CMOS design
- 100pin TQFP
- THC63LVDF84B compatible
- Pin compatible with THC63LVD824

Block Diagram



Pin Out


DE 75
VSYNC 74
HSYNC 73
B17 72
B16 71
GND 70
VCC 69
B15 68
B14 67
B13 66
B12 65
B11 64
B10 63
G17 62
G16 61
G15 60
G14 59
G13 58
GND 57
VCC 56
G12 55
G11 54
G10 53
R17 52
R16 51
LVDS GND 76
RA1- 77
RA1+ 78
RB1- 79
RB1+ 80
LVDS VCC 81
RC1- 82
RC1+ 83
RCLK1- 84
RCLK1+ 85
RD1- 86
RD1+ 87
LVDS GND 88
RA2- 89
RA2+ 90
RB2- 91
RB2+ 92
LVDS VCC 93
RC2- 94
RC2+ 95
RCLK2- 96
RCLK2+ 97
RD2- 98
RD2+ 99
LVDS GND 100
50 R15
49 GND
48 VCC
47 R14
46 R13
45 R12
44 R11
43 R10
42 GND
41 VCC
40 CLKOUT
39 B27
38 B26
37 B25
36 B24
35 B23
34 GND
33 VCC
32 B22
31 B21
30 B20
29 G27
28 GND
27 VCC
26 G26
1 PLL GND
2 PLL VCC
3 GND
4 /PDWN
5 MODE0
6 MODE1
7 GND
8 R/F
9 DRVSEL
10 R20
11 R21
12 R22
13 R23
14 R24
15 VCC
16 GND
17 R25
18 R26
19 R27
20 G20
21 G21
22 G22
23 G23
24 G24
25 G25

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>RA1+, RA1-</td><td>78, 77</td><td>LVDS IN</td><td rowspan="4">The 1st Link. The 1st pixel input data when Dual Link.</td></tr>
<tr><td>RB1+, RB1-</td><td>80, 79</td><td>LVDS IN</td></tr>
<tr><td>RC1+, RC1-</td><td>83, 82</td><td>LVDS IN</td></tr>
<tr><td>RD1+, RD1-</td><td>87, 86</td><td>LVDS IN</td></tr>
<tr><td>RCLK1+, RCLK1-</td><td>85, 84</td><td>LVDS IN</td><td>LVDS Clock Input for 1st Link.</td></tr>
<tr><td>RA2+, RA2-</td><td>90, 89</td><td>LVDS IN</td><td rowspan="4">The 2nd Link. These pins are disabled when Single Link.</td></tr>
<tr><td>RB2+, RB2-</td><td>92, 91</td><td>LVDS IN</td></tr>
<tr><td>RC2+, RC2-</td><td>95, 94</td><td>LVDS IN</td></tr>
<tr><td>RD2+, RD2-</td><td>99, 98</td><td>LVDS IN</td></tr>
<tr><td>RCLK2+, RCLK2-</td><td>97, 96</td><td>LVDS IN</td><td>LVDS Clock Input for 2nd Link.</td></tr>
<tr><td>R17 ~ R10</td><td>52, 51, 50, 47, 46, 45, 44, 43</td><td>OUT</td><td rowspan="3">The 1st Pixel Data Outputs.</td></tr>
<tr><td>G17 ~ G10</td><td>62, 61, 60, 59, 58, 55, 54, 53</td><td>OUT</td></tr>
<tr><td>B17 ~ B10</td><td>72, 71, 68, 67, 66, 65, 64, 63</td><td>OUT</td></tr>
<tr><td>R27 ~ R20</td><td>19, 18, 17, 14, 13, 12, 11, 10</td><td>OUT</td><td rowspan="3">The 2nd Pixel Data Outputs.</td></tr>
<tr><td>G27 ~ G20</td><td>29, 26, 25, 24, 23, 22, 21, 20</td><td>OUT</td></tr>
<tr><td>B27 ~ B20</td><td>39, 38, 37, 36, 35, 32, 31, 30</td><td>OUT</td></tr>
<tr><td>DE</td><td>75</td><td>OUT</td><td>Data Enable Output.</td></tr>
<tr><td>VSYNC</td><td>74</td><td>OUT</td><td>Vsync Output.</td></tr>
<tr><td>HSYNC</td><td>73</td><td>OUT</td><td>Hsync Output.</td></tr>
<tr><td>CLKOUT</td><td>40</td><td>OUT</td><td>Clock Output.</td></tr>
<tr><td>DRVSEL</td><td>9</td><td>IN</td><td>Output Driverbility Select.
<table>
<tr><th>DRVSEL</th><th>clock</th><th>data</th></tr>
<tr><td>H</td><td>8mA</td><td>4mA</td></tr>
<tr><td>L</td><td>4mA</td><td>2mA</td></tr>
</table></td></tr>
<tr><td>R/F</td><td>8</td><td>IN</td><td>Output Clock Triggering Edge Select.
H: Rising edge, L: Falling edge.</td></tr>
<tr><td>MODE1, MODE0</td><td>6, 5</td><td>IN</td><td>Pixel Data Mode.
<table>
<tr><th>MODE1</th><th>MODE0</th><th>Mode</th></tr>
<tr><td>L</td><td>L</td><td>Dual Link (Dual-in/Dual-out)</td></tr>
<tr><td>L</td><td>H</td><td>Single Link(Single-in/Dual-out)</td></tr>
<tr><td colspan="2">other</td><td>Not Available</td></tr>
</table></td></tr>
<tr><td>/PDWN</td><td>4</td><td>IN</td><td>H: Normal operation,
L: Power down (all outputs are pulled to ground)</td></tr>
<tr><td>VCC</td><td>15, 27, 33, 41, 48, 56, 69</td><td>Power</td><td>Power Supply Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>GND</td><td>3, 7, 16, 28, 34, 42, 49, 57, 70</td><td>Ground</td><td>Ground Pins for TTL outputs and digital circuitry.</td></tr>
<tr><td>LVDS VCC</td><td>81,93</td><td>Power</td><td>Power Supply Pins for LVDS inputs.</td></tr>
<tr><td>LVDS GND</td><td>76, 88, 100</td><td>Ground</td><td>Ground Pins for LVDS inputs.</td></tr>
</table>

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Pin Name	Pin #	Type	Description
PLL VCC	2	Power	Power Supply Pin for PLL circuitry.
PLL GND	1	Ground	Ground Pin for PLL circuitry.

Absolute Maximum Ratings [1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V) (≦ 4.0V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V) (≦ 4.0V)
LVDS Receiver Input Voltage	-0.3V ~ (V_{CC} + 0.3V) (≦ 4.0V)
Output Current	-15mA ~ 15mA
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +125°C
Maximum Power Dissipation @+25°C	1.7W

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage		2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage		GND		0.8	V
V_{OH}	High Level Output Voltage	I_{OH}= -2mA, -4mA (data) I_{OH}= -4mA, -8mA (clock)	2.4			V
V_{OL}	Low Level Output Voltage	I_{OL}= 2mA, 4mA (data) I_{OL}= 4mA, 8mA (clock)			0.4	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	μA

LVDS Receiver DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{TH}	Differential Input High Threshold	V_{IC}= 1.2V			100	mV
V_{TL}	Differential Input Low Threshold	V_{IC}= 1.2V	-100			mV
I_{INL}	Input Current	V_{IN}= 2.4V / 0V V_{CC}= 3.6V			±20	μA

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

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Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter	Condition(*)		Typ.	Max.	Units
I_{RCCW}	Receiver Supply Current (Worst Case Pattern)	f_{CLKOUT} = 85MHz	MODE<1:0>=LL CL=8pF, Vcc=3.6V		225	mA
I_{RCCS}	Receiver Power Down Supply Current	/PDWN = L			10	μA

Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = -10°C ~ +70°C

Symbol	Parameter		Min.	Typ.	Max.	Units
t_{RCP}	CLKOUT Period	Dual-in / Dual-out	11.76	t_{RCIP}	40.0	ns
		Single-in / Dual-out	17.85	$2t_{RCIP}$	80.0	ns
t_{RCH}	CLKOUT High Time			$\frac{t_{RCP}}{2}$		ns
t_{RCL}	CKLOUT Low Time			$\frac{t_{RCP}}{2}$		ns
t_{RS}	TTL Data Setup to CLKOUT		$0.3t_{RCP}$-0.5			ns
t_{RH}	TTL Data Hold from CKLOUT		$0.3t_{RCP}$-0.5			ns
t_{TLH}	TTL Low to High Transition Time			2.5	4.0	ns
t_{THL}	TTL High to Low Transition Time			2.5	4.0	ns
t_{SK}	Receiver Skew Margin	CLKIN=85MHz	-0.40		+0.40	ns
		CLKIN=112MHz	-0.25		+0.25	ns
t_{RIP1}	Input Data Position0		$-t_{SK}$	0.0	$+t_{SK}$	ns
t_{RIP0}	Input Data Position1		$\frac{t_{RCIP}}{7} - t_{SK}$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP6}	Input Data Position2		$2\frac{t_{RCIP}}{7} - t_{SK}$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP5}	Input Data Position3		$3\frac{t_{RCIP}}{7} - t_{SK}$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP4}	Input Data Position4		$4\frac{t_{RCIP}}{7} - t_{SK}$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP3}	Input Data Position5		$5\frac{t_{RCIP}}{7} - t_{SK}$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RIP2}	Input Data Position6		$6\frac{t_{RCIP}}{7} - t_{SK}$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7} + t_{SK}$	ns
t_{RPLL}	Phase Lock Loop Set				10.0	ms
t_{RCIP}	CLKIN Period		8.92		40.0	ns
t_{CK12}	Skew Time between RCLK1 and RCLK2				$\pm 0.3t_{RCIP}$	ns

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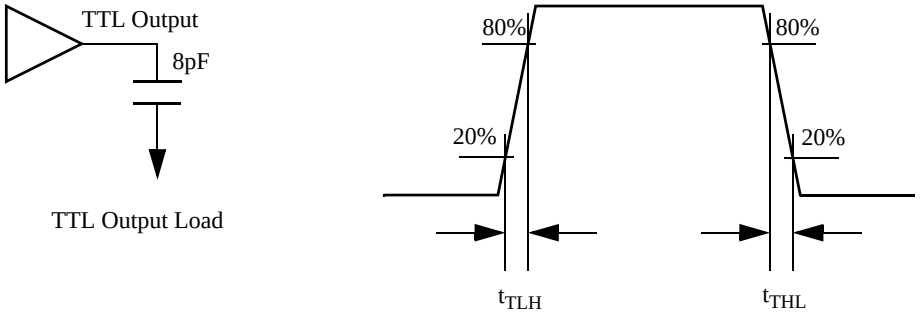
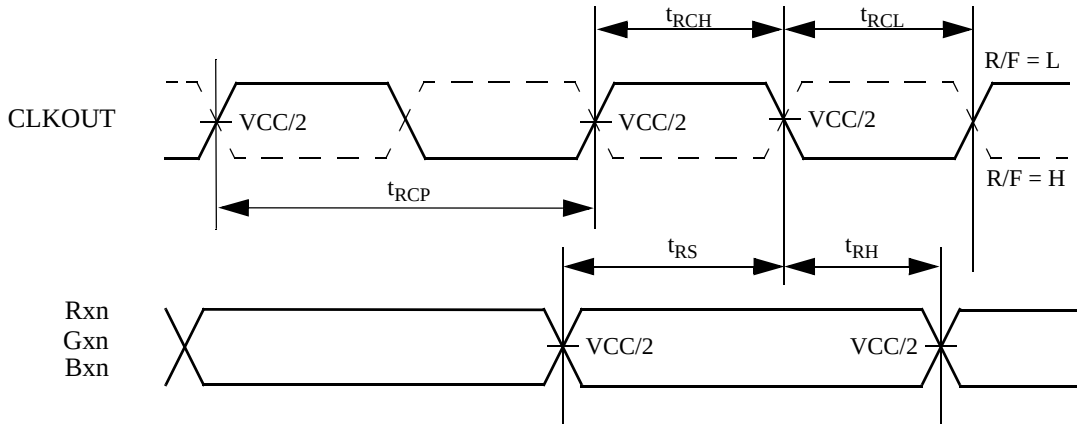
AC Timing Diagrams

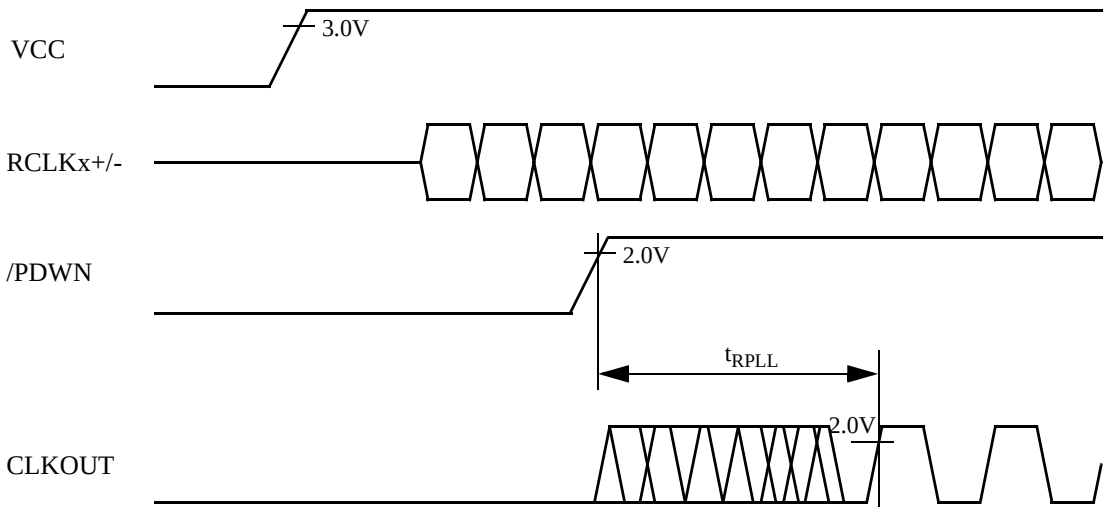
TTL Outputs





x = 1,2
n = 0~7

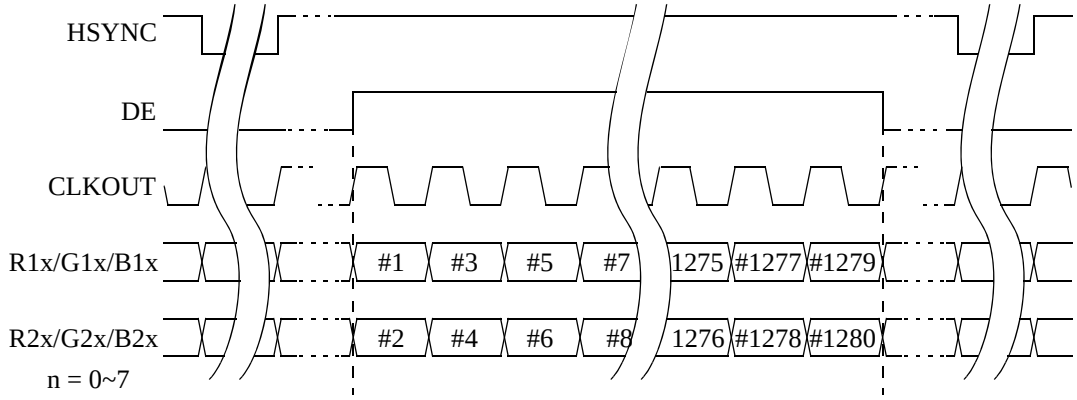
Phase Lock Loop Set Time

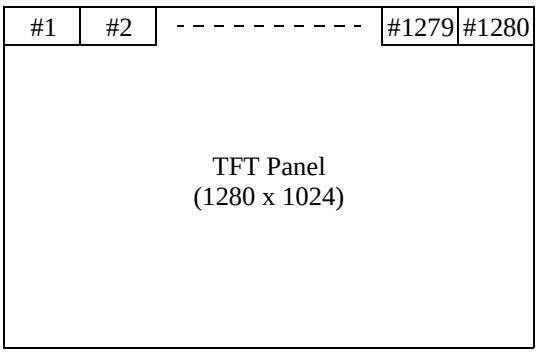


Pixel Map Table for Single/Dual Link

1st Pixel Data				2nd Pixel Data			
824A TTLOutputPin	TFT Panel Data			824A TTLOutputPin	TFT Panel Data		
		24Bit	18Bit			24Bit	18Bit
R10	LSB	R10	-	R20	LSB	R20	-
R11		R11	-	R21		R21	-
R12		R12	R10	R22		R22	R20
R13		R13	R11	R23		R23	R21
R14		R14	R12	R24		R24	R22
R15		R15	R13	R25		R25	R23
R16		R16	R14	R26		R26	R24
R17	MSB	R17	R15	R27	MSB	R27	R25
G10	LSB	G10	-	G20	LSB	G20	-
G11		G11	-	G21		G21	-
G12		G12	G10	G22		G22	G20
G13		G13	G11	G23		G23	G21
G14		G14	G12	G24		G24	G22
G15		G15	G13	G25		G25	G23
G16		G16	G14	G26		G26	G24
G17	MSB	G17	G15	G27	MSB	G27	G25
B10	LSB	B10	-	B20	LSB	B20	-
B11		B11	-	B21		B21	-
B12		B12	B10	B22		B22	B20
B13		B13	B11	B23		B23	B21
B14		B14	B12	B24		B24	B22
B15		B15	B13	B25		B25	B23
B16		B16	B14	B26		B26	B24
B17	MSB	B17	B15	B27	MSB	B27	B25

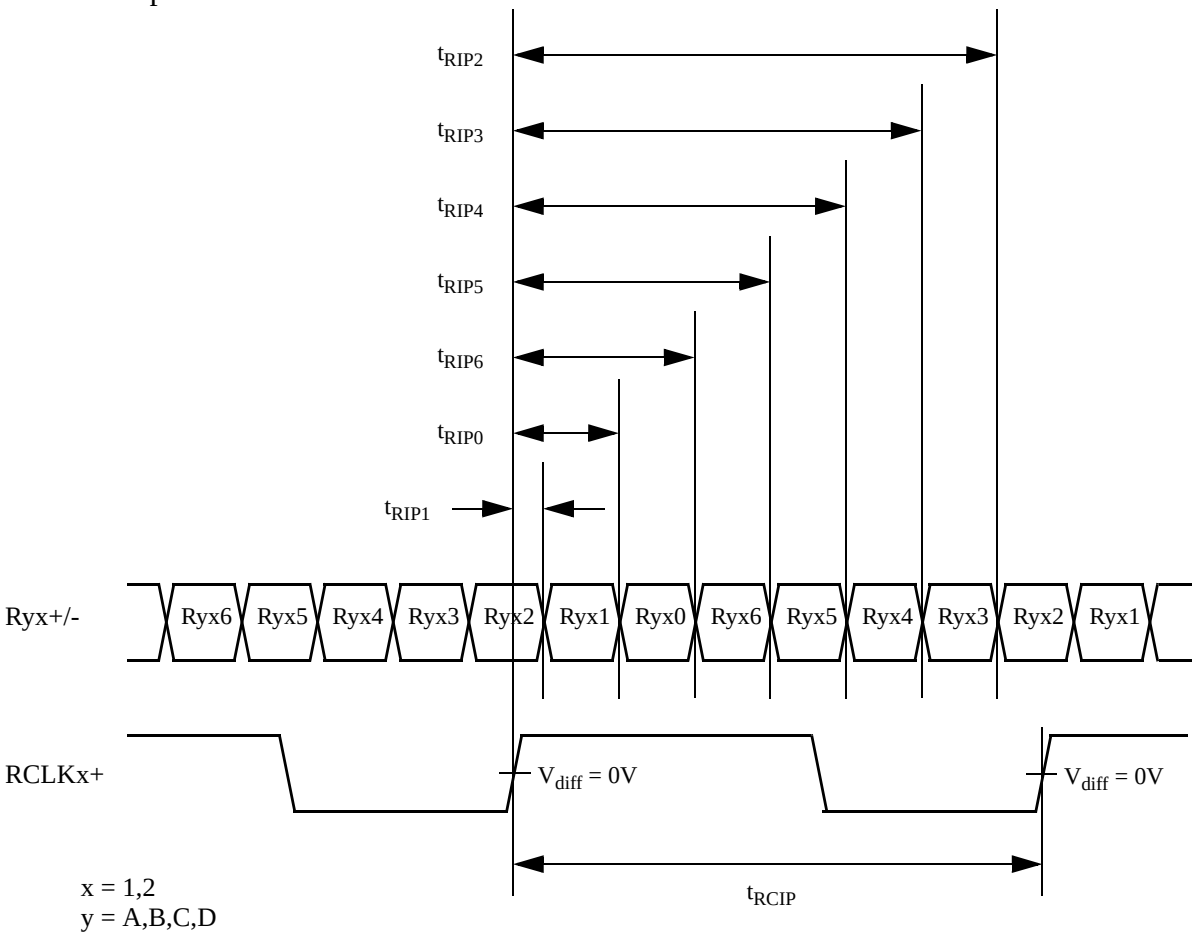
824A TTL Data Output Timing for Single/Dual Link
Example : SXGA(1280 x 1024)



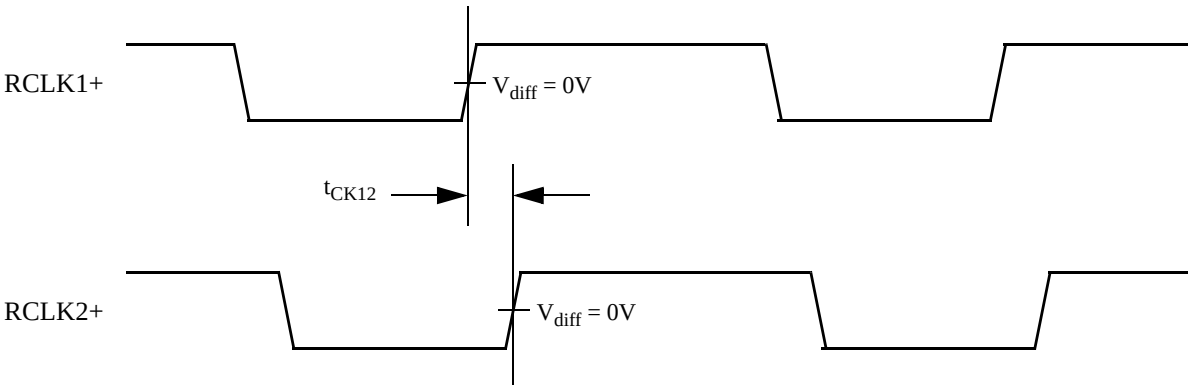


AC Timing Diagrams

LVDS Inputs

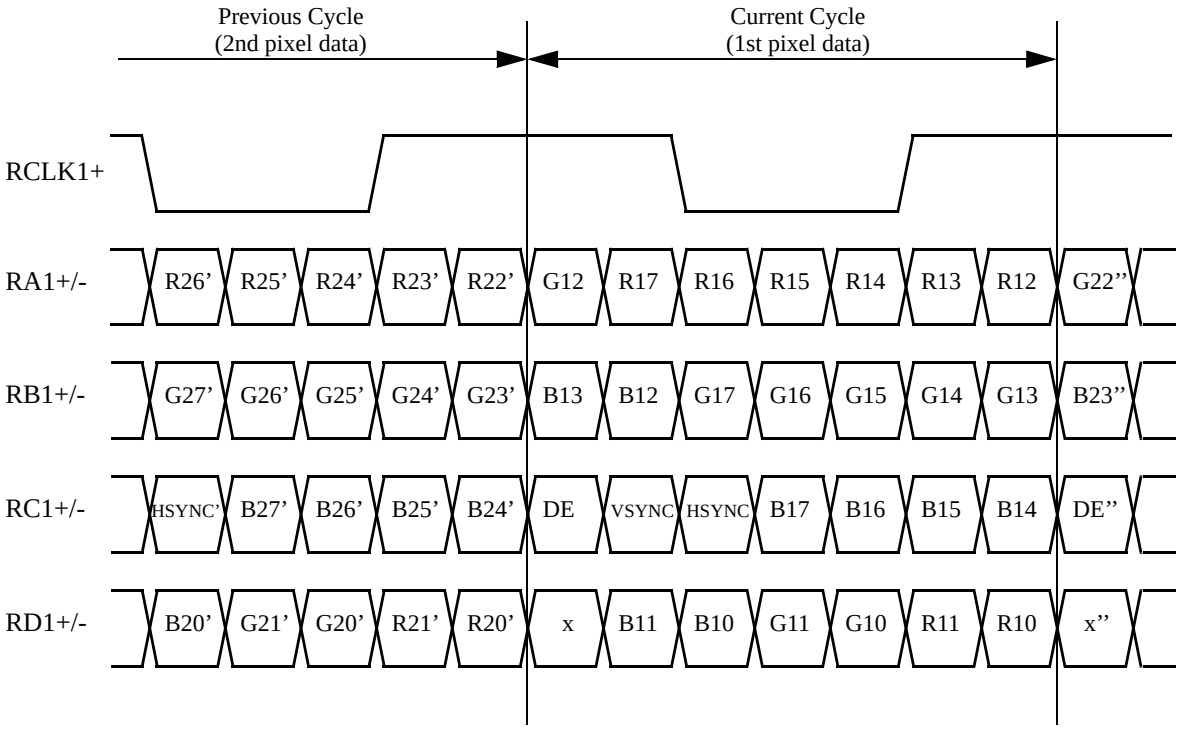


x = 1,2
y = A,B,C,D



Note:
V_{diff} = (Ryx+) - (Ryx-), (RCLKx+) - (RCLKx-)

LVDS Data Inputs Timing Diagrams in Single Link



LVDS Data Inputs Timing Diagrams in Dual Link

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Note

1)Power On Sequence

Power on LVDS-Tx after THC63LVD824A. If it is not avoidable, please contact to

mspsupport@thine.co.jp (for FAE mailing list)

2)Cable Connection and Disconnection

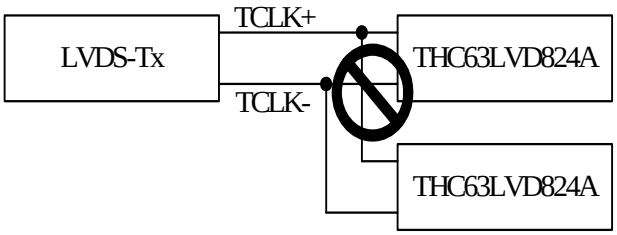
Don't connect and disconnect the LVDS cable , when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which LVDS-Tx and THC63LVD824A on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

4)Multi Drop Connection

Multi drop connection is not recommended.



5)Asynchronous use

Asynchronous use such as following systems are not recommended. If it is not avoidable, please contact to

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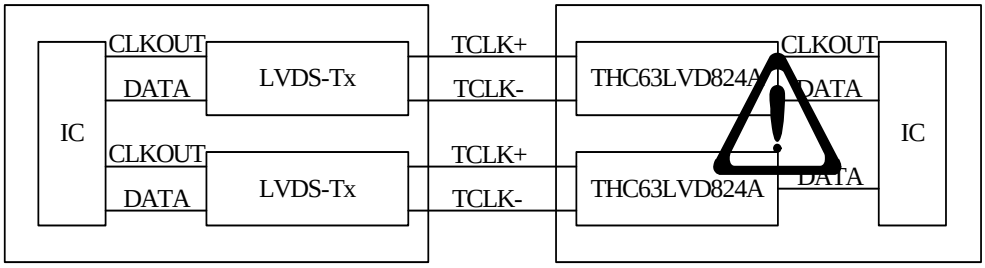
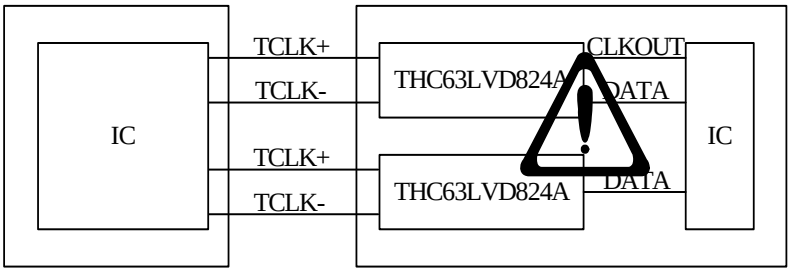
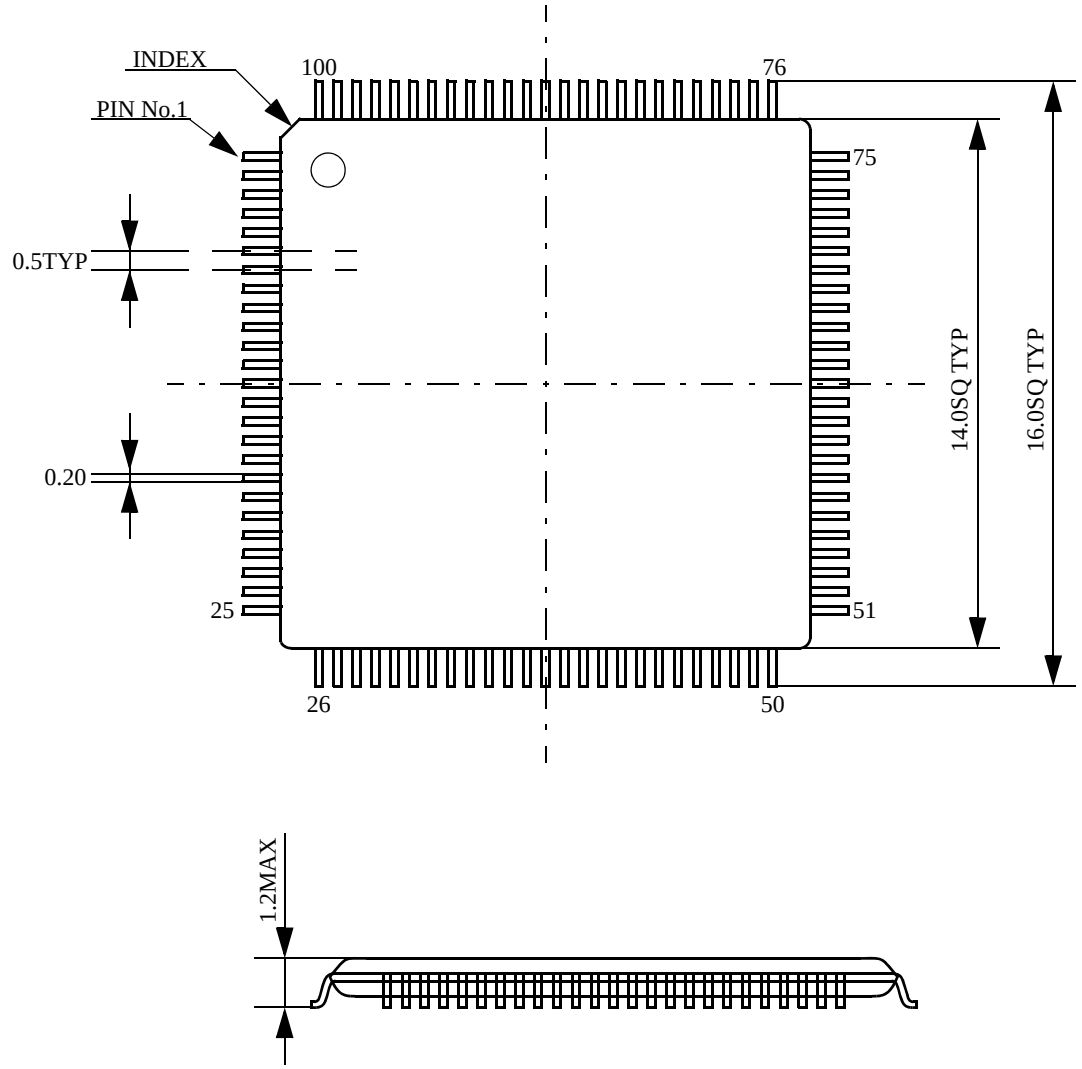




Package



UNITS:mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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