TDA7255V

ASK/FSK 434 MHz Wireless Transceiver

Data Sheet

Revision 1.1, 2010-11-10

Wireless Sense & Control

Edition 2010-11-10

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 1.1, 2010-11-10	
	Just minor changes

Trademarks of Infineon Technologies AG

AURIX™, BlueMoon™, COMNEON™, C166™, CROSSAVE™, CanPAK™, CIPOS™, CoolMOS™, CoolSET™, CORECONTROL™, DAVE™, EasyPIM™, EconoBRIDGE™, EconoDUAL™, EconoPACK™, EconoPIM™, EiceDRIVER™, EUPEC™, FCOS™, HITFET™, HybridPACK™, ISOFACE™, I²RF™, IsoPACK™, MIPAQ™, ModSTACK™, my-d™, NovalithIC™, OmniTune™, OptiMOS™, ORIGA™, PROFET™, PRO-SIL™, PRIMARION™, PrimePACK™, RASIC™, ReverSave™, SatRIC™, SIEGET™, SINDRION™, SMARTi™, SmartLEWIS™, TEMPFET™, thinQ!™, TriCore™, TRENCHSTOP™, X-GOLD™, XMM™, X-PMU™, XPOSYS™.

Other Trademarks

Advance Design System™ (ADS) of Agilent Technologies, AMBA™, ARM™, MULTI-ICE™, PRIMECELL™, REALVIEW™, THUMB™ of ARM Limited, UK. AUTOSAR™ is licensed by AUTOSAR development partnership. Bluetooth™ of Bluetooth SIG Inc. CAT-iq™ of DECT Forum. COLOSSUS™, FirstGPS™ of Trimble Navigation Ltd. EMV™ of EMVCo, LLC (Visa Holdings Inc.). EPCOS™ of Epcos AG. FLEXGO™ of Microsoft Corporation. FlexRay™ is licensed by FlexRay Consortium. HYPERTERMINAL™ of Hilgraeve Incorporated. IEC™ of Commission Electrotechnique Internationale. IrDA™ of Infrared Data Association Corporation. ISO™ of INTERNATIONAL ORGANIZATION FOR STANDARDIZATION. MATLAB™ of MathWorks, Inc. MAXIM™ of Maxim Integrated Products, Inc. MICROTEC™, NUCLEUS™ of Mentor Graphics Corporation. Mifare™ of NXP. MIPI™ of MIPI Alliance, Inc. MIPS™ of MIPS Technologies, Inc., USA. muRata™ of MURATA MANUFACTURING CO., MICROWAVE OFFICE™ (MWO) of Applied Wave Research Inc., OmniVision™ of OmniVision Technologies, Inc. Openwave™ Openwave Systems Inc. RED HAT™ Red Hat, Inc. RFMD™ RF Micro Devices, Inc. SIRIUS™ of Sirius Sattelite Radio Inc. SOLARIS™ of Sun Microsystems, Inc. SPANSION™ of Spansion LLC Ltd. Symbian™ of Symbian Software Limited. TAIYO YUDEN™ of Taiyo Yuden Co. TEAKLITE™ of CEVA, Inc. TEKTRONIX™ of Tektronix Inc. TOKO™ of TOKO KABUSHIKI KAISHA TA. UNIX™ of X/Open Company Limited. VERILOG™, PALLADIUM™ of Cadence Design Systems, Inc. VLYNQ™ of Texas Instruments Incorporated. VXWORKS™, WIND RIVER™ of WIND RIVER SYSTEMS, INC. ZETEX™ of Diodes Zetex Limited.

Last Trademarks Update 2010-06-09

Table of Contents

1 Product Description

1.1 Overview

The TDA7255V is an ASK/FSK single-channel transceiver for 433 - 435 MHz frequency band in a tiny VQFN-40 package. Due to the very high level of integration the device requires only a few external components. The extreme low current consumption in receive, transmit and especially in power down mode and the wide supply voltage range make TDA7255V the ideal choice for small, battery driven applications.

The device contains a low noise amplifier (LNA), a double balanced mixer, a fully integrated VCO, a PLL synthesizer, a crystal oscillator with FSK modulator, a limiter with RSSI generator, a FSK demodulator, a data filter, a data comparator (slicer), a positive and a negative data peak detector, a highly efficient power amplifier and a complex digital timing and control unit with I^2C/3-wire microcontroller interface. Additionally there is a power down feature to save battery power.

The transmit section uses direct ASK modulation by switching the power amplifier, and crystal oscillator detuning for FSK modulation. The necessary detuning load capacitors are external. The capacitors for fine tuning are integrated. The receive section is using a novel single-conversion/direct-conversion scheme that is combining the advantages of both receive topologies. The IF is contained on the chip, no RF channel filters are necessary as the channel filter is also on the chip.

The self-polling logic can be used to let the device operate autonomously as a master for a decoding microcontroller.

1.2 Features

- FSK and ASK modulation and demodulation capability without external circuitry changes, FM demodulation capability
- Frequency range: 433 to 435 MHz
- Sensitivity FSK typically -115 dBm at 4 kbit/s data rate
- Sensitivity ASK typically -112 dBm at 4 kbit/s data rate
- Transmit power up to +13 dBm
- Low supply current (I_s = 9 mA typ. in receive mode, I_s = 13,5 mA typ. in transmit mode (both at 3 V supply voltage, 25°C)
- Very low supply current in power down mode (5 nA typ.)
- Supply voltage range: 2.1 V to 5.5 V
- Data rates up to 100 kbit/s Manchester encoded
- Fully integrated PLL synthesizer including VCO and loop filter on-chip with on-chip crystal oscillator tuning
- Differential receive signal path completely on-chip, therefore no external filters are necessary
- On-chip low pass channel select and data filter with tuneable bandwidth
- Data slicer with self-adjusting threshold and 2 peak detectors
- Self-polling logic with adjustable duty cycle and ultrafast data rate detection and timer mode providing periodical interrupt
- Adjustable LNA gain
- Digital RSSI and battery voltage readout
- Clock Out Pin for external microcontroller
- I^2C/3-wire microcontroller interface, working at max. 400 kbit/s
- Operating temperature range -40°C to +85°C
- 5.5 x 6.5 mm small VQFN-40 package

1.3 Application

The TDA7255V is targeted specifically at highly size-sensitive industrial and consumer applications such as small home automation or security and alarm systems.

Main applications:

- Bi-directional remote control systems
- Home automation systems
- Lighting control
- Security and alarm systems
- Industrial control
- Remote keyless entry systems
- Low bit-rate communication systems

1.4 Ordering Information

Type	Ordering Code	Package
TDA7255V	SP000698114	PG-VQFN-40-8

1.5 Package Outlines

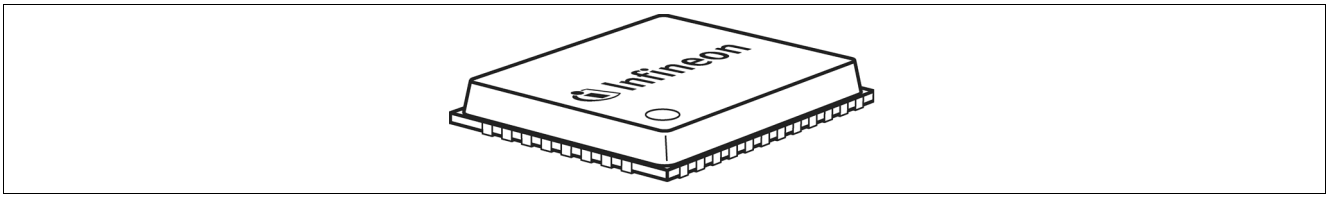


Figure 1 Package PG-VQFN-40-8

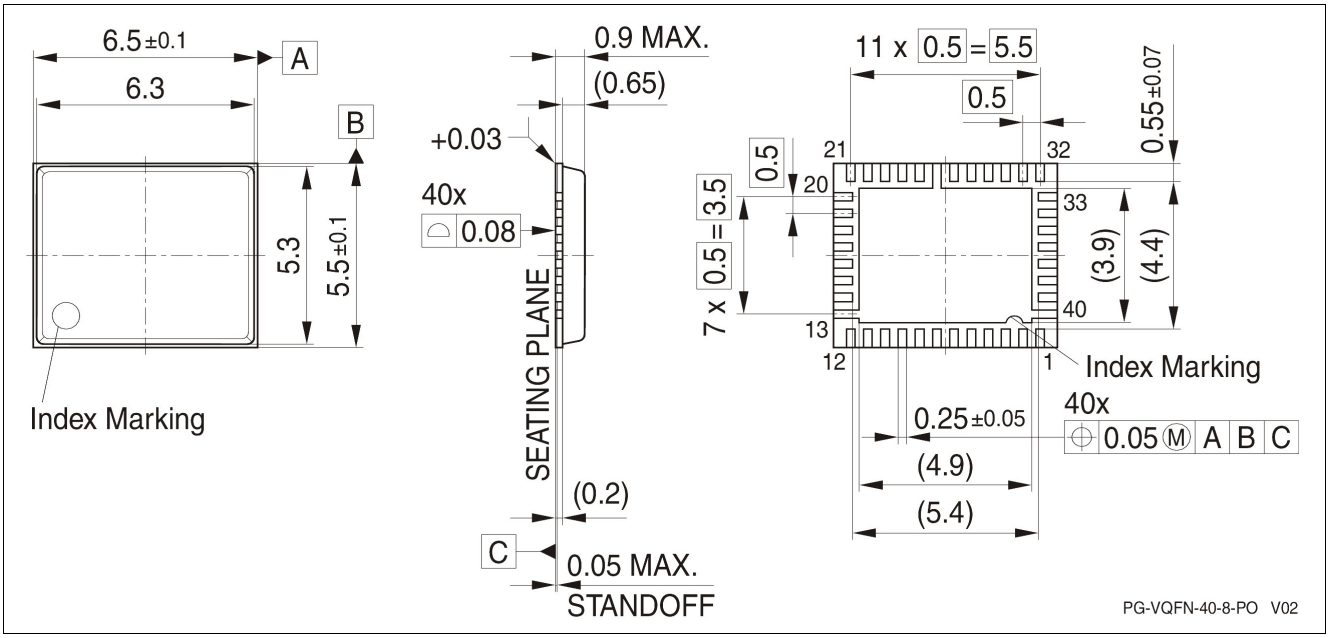


Figure 2 PG-VQFN-40-8 Package Outlines

2 Functional Description

2.1 Pin Configuration

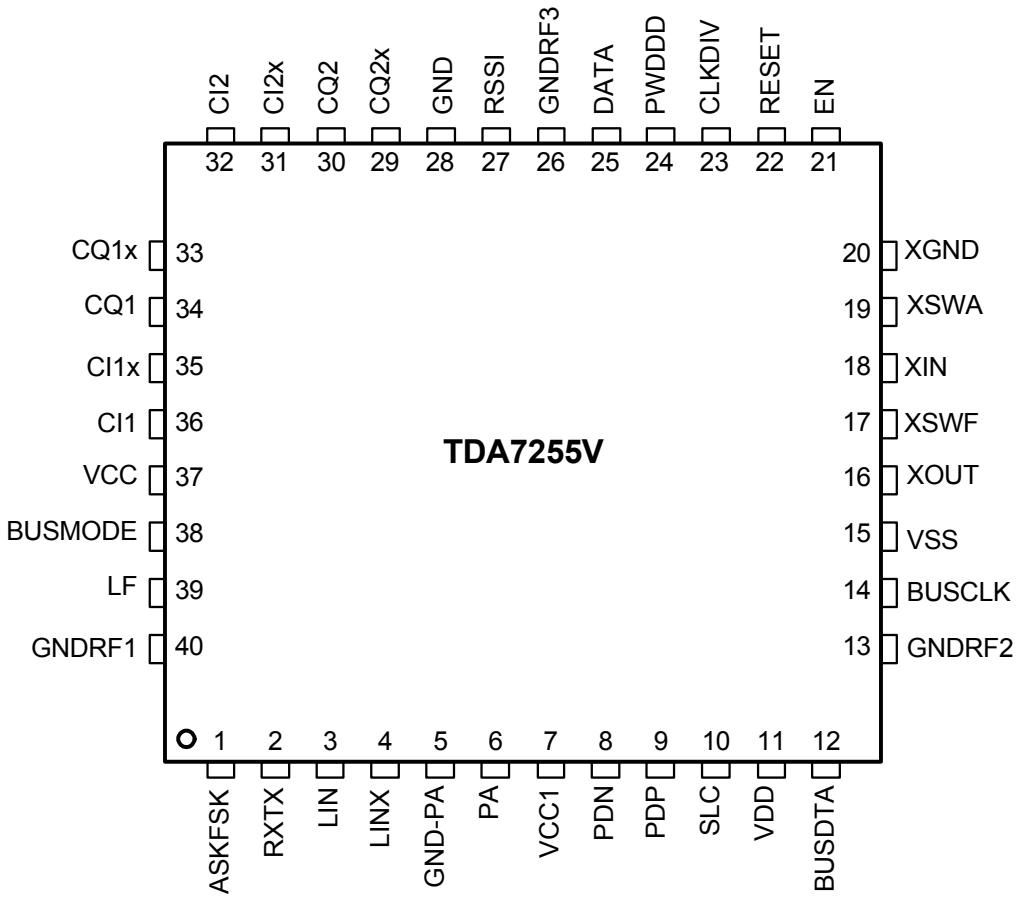


Figure 3 Pin Configuration TDA7255V

2.2 Pin Definitions and Functions

Table 1 Pin Definition and Function

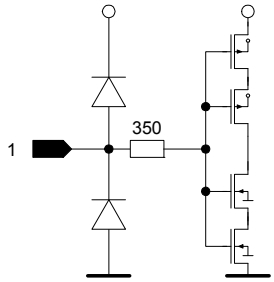
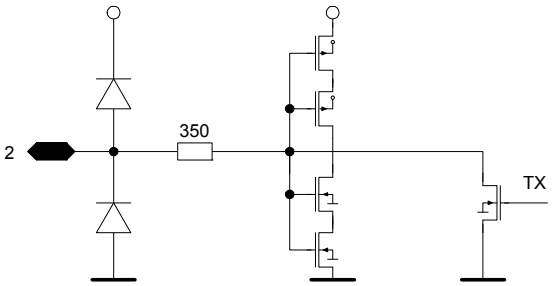
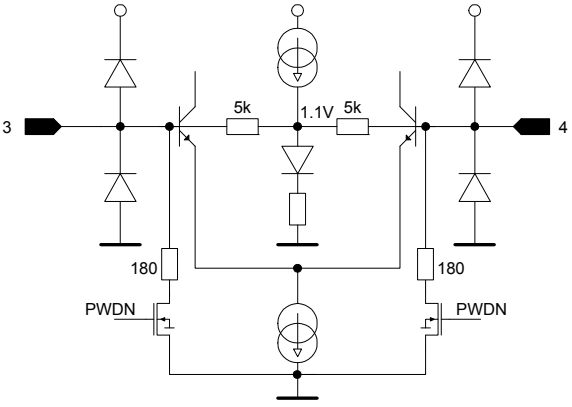
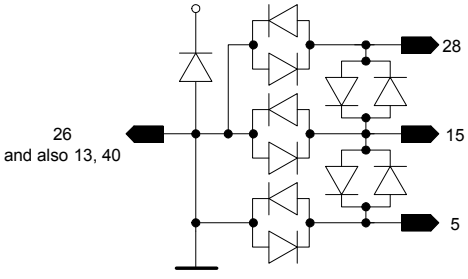
Ball No.	Name	Pin Type	Buffer Type	Function
1	ASKFSK			ASK/FSK-Mode Switch Input High = ASK Low = FSK
2	RXTX			RX/TX-Mode Switch Input/Output High = RX Low = TX
3	LNI			RF Input to Differential Low Noise Amplifier (LNA)
4	LNIX		See Pin 3	Complementary RF Input to Differential LNA
5	GND-PA			Ground Return for Power Amplifier (PA) Driver Stage

Table 1 Pin Definition and Function (cont'd)

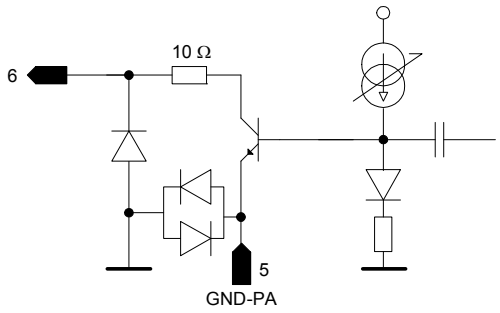
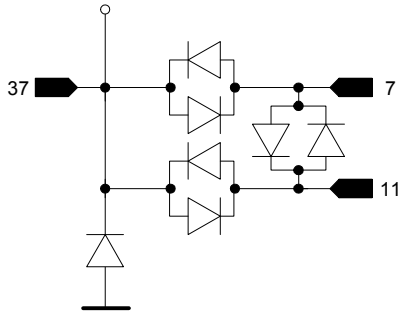
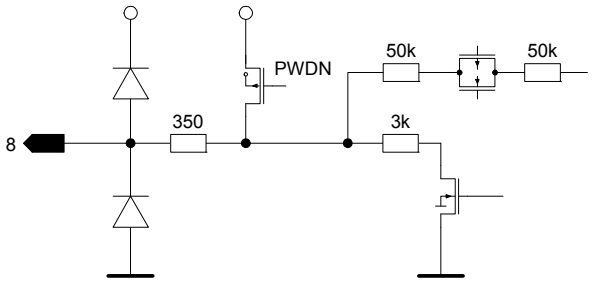
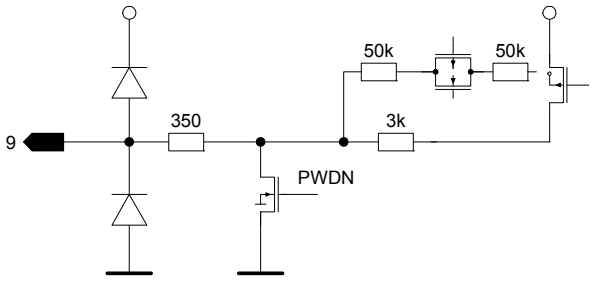
Ball No.	Name	Pin Type	Buffer Type	Function
6	PA			PA Output Stage
7	VCC1			Supply for LNA and PA
8	PDN			Output of the Negative Peak Detector
9	PDP			Output of the Positive Peak Detector

Table 1 Pin Definition and Function (cont'd)

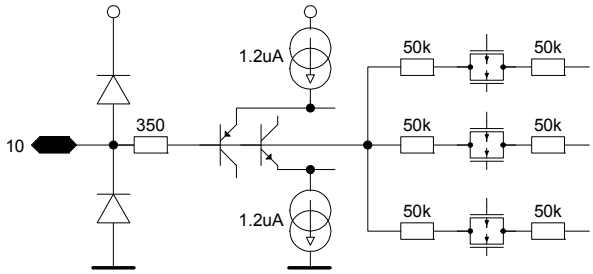
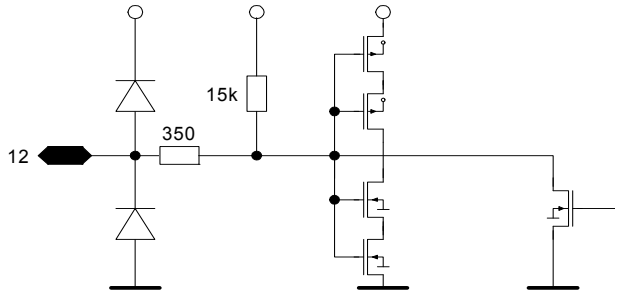
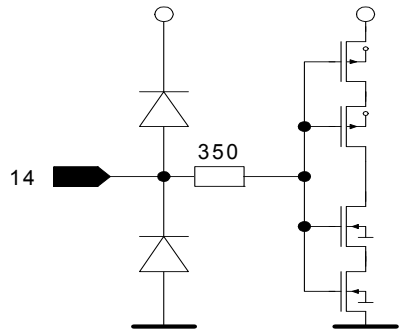
Ball No.	Name	Pin Type	Buffer Type	Function
10	SLC			Slicer Level for the Data Slicer
11	VDD		See Pin 7	Digital Supply A 10 Ω serial resistor in the VDD supply line is strongly recommended; see also **Chapter 4.4**
12	BUSDTA			Bus Data In/Output
13	GNDRF2		See Pin 5	Ground Return for RF Except PA
14	BUSCLK			Bus Clock Input
15	VSS		See Pin 5	Ground for Digital Section

Table 1 Pin Definition and Function (cont'd)

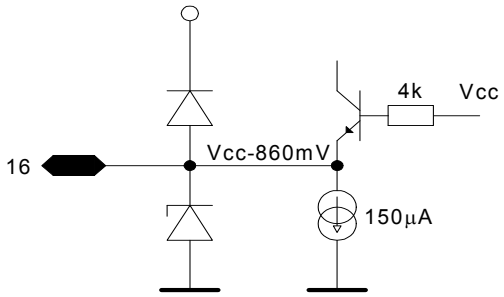
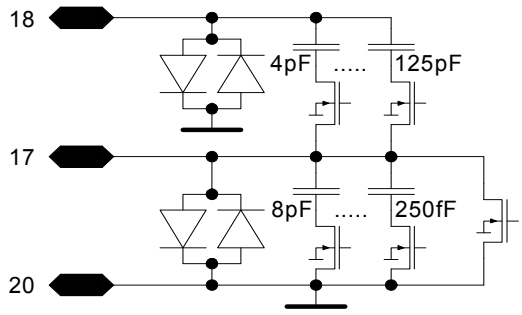
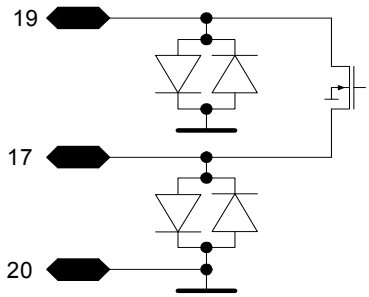
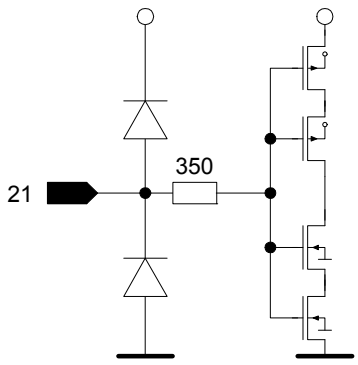
Ball No.	Name	Pin Type	Buffer Type	Function
16	XOUT			Crystal Oscillator Output Can also be used as external reference frequency input
17	XSWF			FSK Modulation Switch
18	XIN		See Pin 17	Ground for Digital Section
19	XSWA			ASK Modulation/FSK Center Frequency Switch
20	XGND		See Pin 19	Crystal Oscillator Ground Return
21	EN			3-Wire Bus Enable Input, Active Low

Table 1 Pin Definition and Function (cont'd)

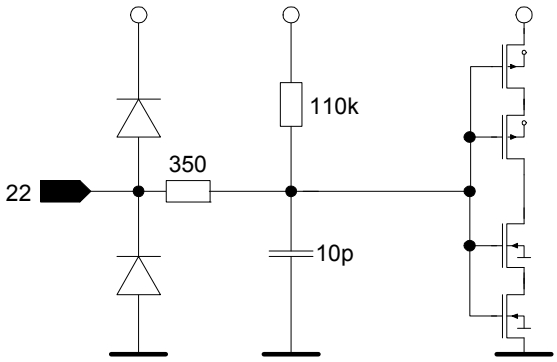
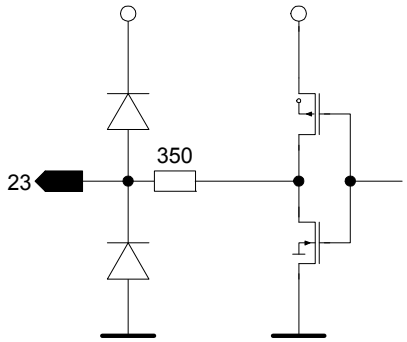
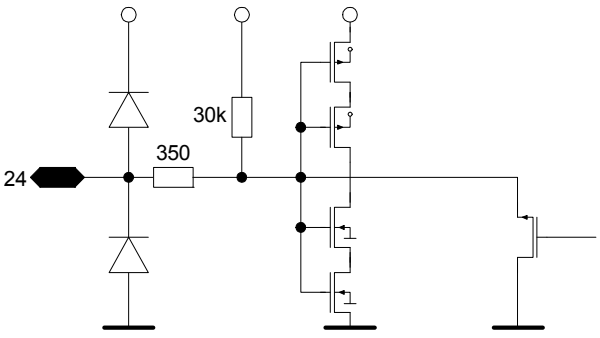
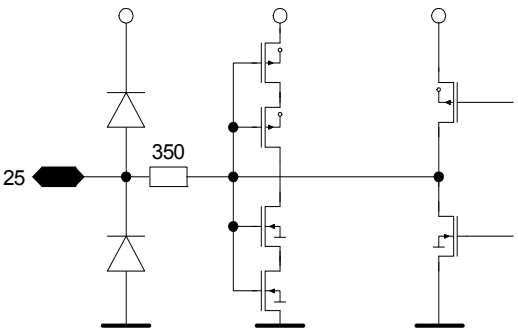
Ball No.	Name	Pin Type	Buffer Type	Function
22	RESET			Reset of the Entire System (to Default Values) Active Low
23	CLKDIV			Clock Output
24	PWDDD			Power Down Input (Active High), Data Detect Output (Active Low)
25	DATA			TX Data Input, RX Data Output (RX Powerdown: Pin 25 @ GND)
26	GNDRF3		See Pin 5	Ground Return for RF except PA

Table 1 Pin Definition and Function (cont'd)

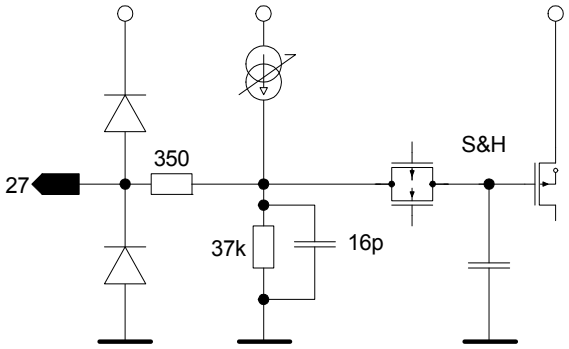
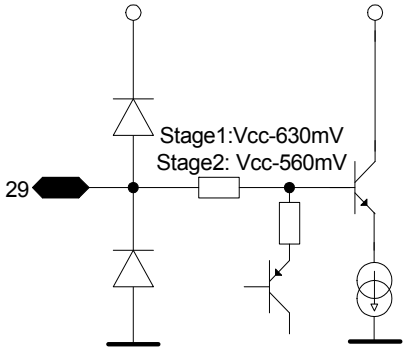
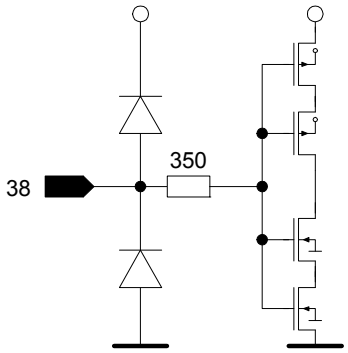
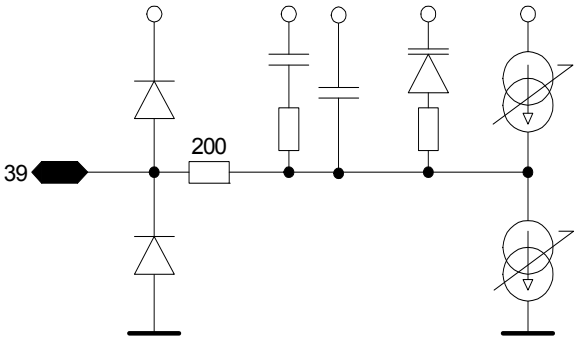
Ball No.	Name	Pin Type	Buffer Type	Function
27	RSSI			RSSI Output
28	GND		See Pin 5	Analog Ground
29	CQ2x			Pin for External Capacitor Q-channel, stage 2
30	CQ2		See Pin 29	Pin for External Capacitor Q-channel, stage 2
31	CI2x		See Pin 29	Pin for External Capacitor I-channel, stage 2
32	CI2		See Pin 29	Pin for External Capacitor I-channel, stage 2
33	CQ1x		See Pin 29	Pin for External Capacitor Q-channel, stage 1
34	CQ1		See Pin 29	Pin for External Capacitor Q-channel, stage 1
35	CI1x		See Pin 29	Pin for External Capacitor I-channel, stage 1
36	CI1		See Pin 29	Pin for External Capacitor I-channel, stage 1
37	VCC		See Pin 7	Analog Supply Antiparallel diodes between VCC, VCC1, VDD

Table 1 Pin Definition and Function (cont'd)

Ball No.	Name	Pin Type	Buffer Type	Function
38	BUSMODE			Bus Mode Selection I^2C/3 wire bus mode selection
39	LF			Loop Filter and VCO Control Voltage
40	GNDRF1		See Pin 5	Ground Return for LNA

2.3 Functional Block Diagram

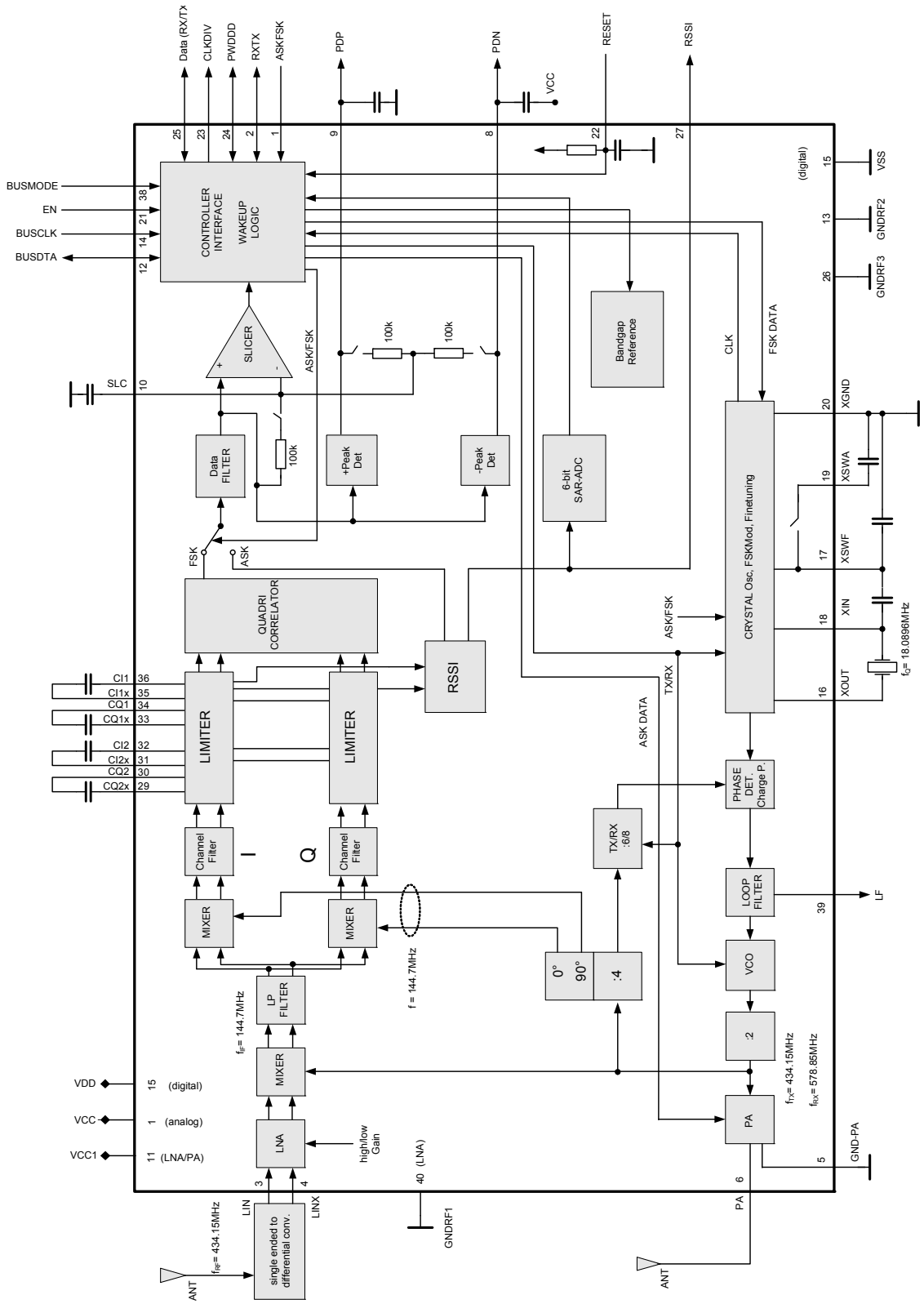


Figure 4 Main Block Diagram

2.4 Functional Block Description

2.4.1 Power Amplifier (PA)

The power amplifier is operating in C-mode. It can be used in either high or low power mode. In high-power mode the transmit power is approximately +13 dBm into 50 Ω at 5 V and +6 dBm at 2.1 V supply voltage. In low power mode the transmit power is approximately +11 dBm at 5 V and -32 dBm at 2.1 V supply voltage using the same matching network. The transmit power is controlled by the D0-bit of the CONFIG register (sub-address 00H) as shown in the following **Table 2**. The default output power mode is high power mode.

Table 2 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D0	PA_PWR	0 = Low TX Power, 1 = High TX Power	1

In case of ASK modulation the power amplifier is turned fully on and off by the transmit baseband data, i.e. 100% On-Off-Keying.

2.4.2 Low Noise Amplifier (LNA)

The LNA is an on-chip cascode amplifier with a voltage gain of 15 to 20 dB and symmetrical inputs. It is possible to reduce the gain to 0 dB via logic.

Table 3 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D4	LNA_GAIN	0 = Low Gain, 1 = High Gain	1

2.4.3 Downconverter 1st Mixer

The Double Balanced 1st Mixer converts the input frequency (RF) in the range of 434-435 MHz down to the intermediate frequency (IF) at approximately 144 MHz. The local oscillator frequency is generated by the PLL synthesizer that is fully implemented on-chip as described in **Chapter 2.4.5**. This local oscillator operates at approximately 578 MHz in receive mode providing the above mentioned IF frequency of 144 MHz. The mixer is followed by a low pass filter with a corner frequency of approximately 175 MHz in order to prevent RF and LO signals from appearing in the 144 MHz IF signal.

2.4.4 Downconverter 2nd I/Q Mixers

The Low pass filter is followed by 2 mixers (inphase I and quadrature Q) that convert the 144 MHz IF signal down to zero-IF. These two mixers are driven by a signal that is generated by dividing the local oscillator signal by 4, thus equalling the IF frequency.

2.4.5 PLL Synthesizer

The Phase Locked Loop synthesizer consists of two VCOs (i.e. transmit and receive VCO), a divider by 4, an asynchronous divider chain with selectable overall division ratio, a phase detector with charge pump and a loop filter and is fully implemented on-chip. The VCOs are including spiral inductors and varactor diodes. The center frequency of the transmit VCO is 868 MHz, the center frequency of the receive VCO is 1156 MHz.

Generally in receive mode the relationship between local oscillator frequency f_{osc}, the receive RF frequency f f_{RF} and the IF frequency f f_{IF} and thus the frequency that is applied to the I/Q Mixers is given in the following formula:

$$\frac{f_{osc}}{2} = 4/3\, f_{RF} = 4\, f_{IF} \quad (1)$$

The VCO signal is applied to a divider by 2 and afterwards by 4 which is producing approximately 144 MHz signals in quadrature. The overall division ratio of the divider chain following the divider by 2 and 4 is 6 in transmit mode and 8 in receive mode as the nominal crystal oscillator frequency is 18.083 MHz. The division ratio is controlled by the RxTx pin (pin 2) and the D10 bit in the CONFIG register.

2.4.6 I/Q Filters

The I/Q IF to zero-IF mixers are followed by baseband 6th order low pass filters that are used for RF-channel filtering.

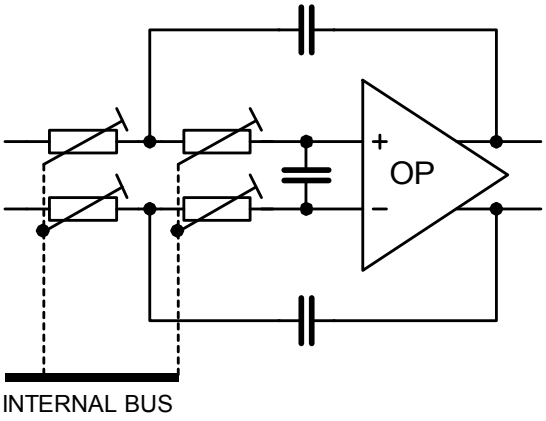


Figure 5 One I/Q Filter Stage

The bandwidth of the filters is controlled by the values set in the filter-register. It can be adjusted between 50 and 350 kHz in 50 kHz steps via the bits D1 to D3 of the LPF register (sub-address 03H).

2.4.7 I/Q Limiters

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80 dB each in the frequency range of 100 Hz up to 350 kHz. Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

2.4.8 FSK Demodulator

The output differential signals of the I/Q limiters are fed to a quadrature correlator circuit that is used to demodulate frequency shift keyed (FSK) signals. The demodulator gain is 2.4 mV/kHz, the maximum frequency deviation is ±300 kHz as shown in **Figure 6** below.

The demodulated signal is applied to the ASK/FSK mode switch which is connected to the input of the data filter. The switch can be controlled by the ASKFSK pin (pin 1) and via the D11 bit in the CONFIG register.

The modulation index m must be significantly larger than 2 and the deviation at least larger than 25 kHz for correct demodulation of the signal.

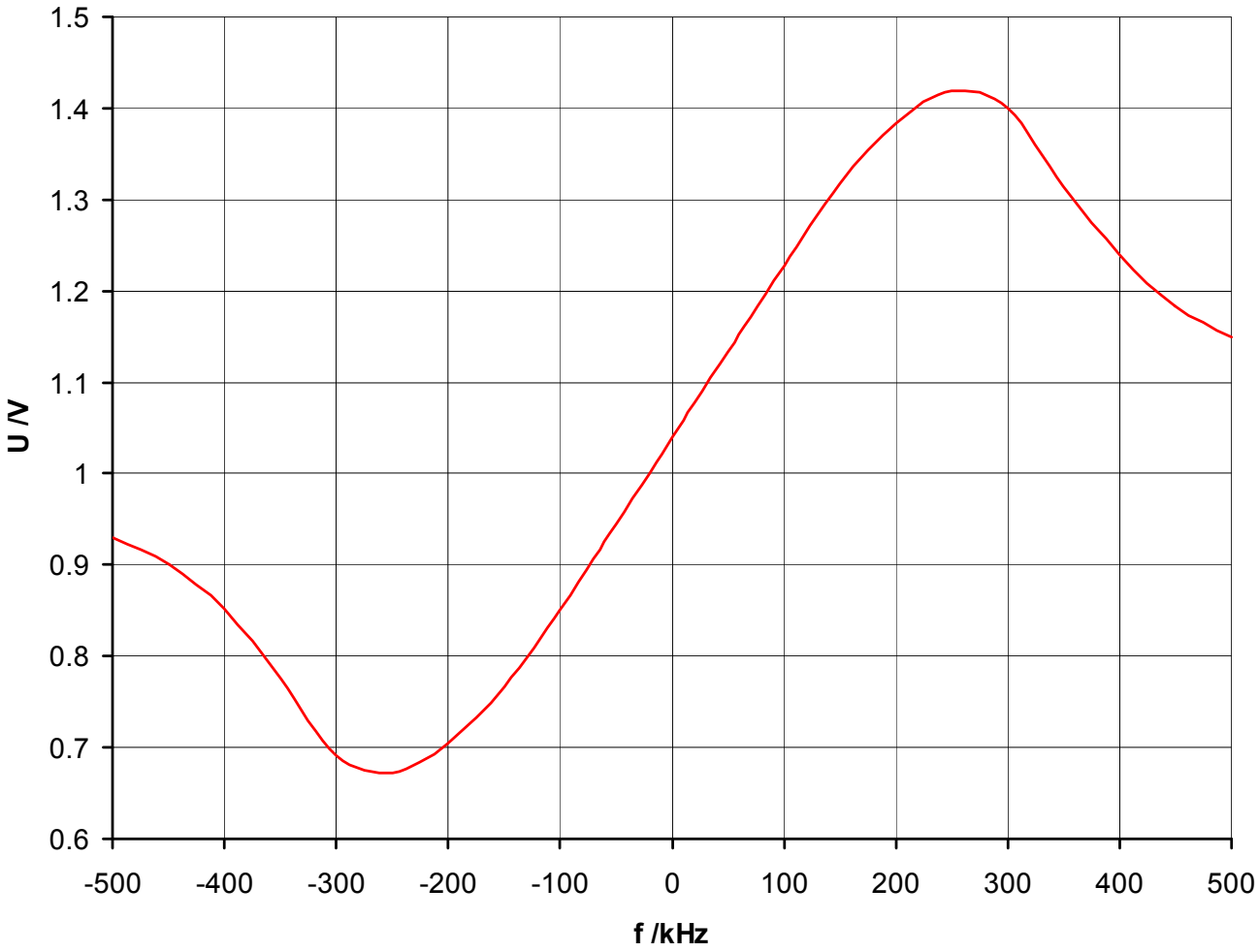


Figure 6 Quadricorrelator Demodulation Characteristic

2.4.9 Data Filter

The 2-pole data filter has a Sallen-Key architecture and is implemented fully on-chip. The bandwidth can be adjusted between approximately 5 kHz and 102 kHz via the bits D4 to D7 of the LPF register as shown in **Table 29**.

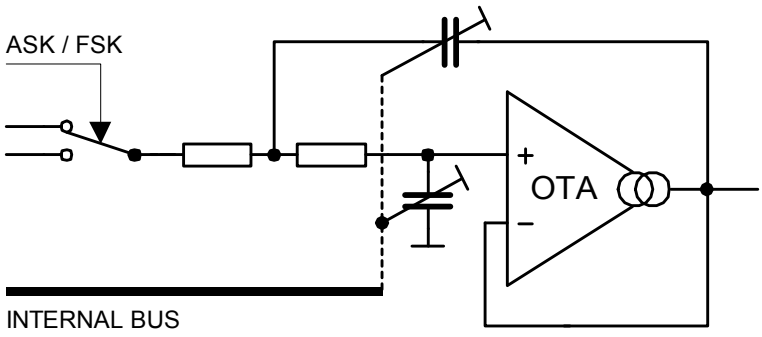


Figure 7 Data Filter Architecture

2.4.10 Data Slicer

The data slicer is a fast comparator with a bandwidth of 100 kHz. The self-adjusting threshold is generated by a RC-network (LPF) or by use of one or both peak detectors depending on the baseband coding scheme as described in **Chapter 3.6**. This can be controlled by the D15 bit of the CONFIG register as shown in the following table.

Table 4 Sub Address 00H: CONFIG

Bit	Function	Description	Default
D15	SLICER	0 = Lowpass Filter, 1 = Peak Detector	0

2.4.11 Peak Detectors

Two separate Peak Detectors are available. They are generating DC voltages in a fast-attack and slow-release manner that are proportional to the positive and negative peak voltages appearing in the data signal. These voltages may be used to generate a threshold voltage for non-Manchester encoded signals, for example. The time-constant of the fast-attack/slow-release action is determined by the RC network with external capacitor.

2.4.12 Crystal Oscillator

The reference oscillator is an NIC oscillator type (Negative Impedance Converter) with a crystal operating in serial resonance. The nominal operating frequency of 18.089583 MHz and the frequencies for FSK modulation can be adjusted via 3 external capacitors. Via microcontroller and bus interface the chip-internal capacitors can be used for fine-tuning of the nominal and the FSK modulation frequencies. This fine-tuning of the crystal oscillator allows to eliminate frequency errors due to crystal or component tolerances.

2.4.13 Bandgap Reference Circuitry and Powerdown

A Bandgap Reference Circuit provides a temperature stable 1.2 V reference voltage for the device. A power down mode is available to switch off all subcircuits that are controlled by the bidirectional Powerdown & DataDetect PWDDD pin (pin 24) as shown in the following table. Power down mode can either be activated by pin 24 or bit D14 in Register 00h. In power down mode also pin 25 (DATA) is affected (see **Chapter 2.4.18**).

Table 5 PWDDD Pin Operating States

PWDDD	Operating State
VDD	Powerdown Mode
Ground/VSS	Device On

2.4.14 Timing and Data Control Unit

The timing and data control unit contains a wake-up logic unit, an I²C/3-wire microcontroller interface, a “data valid” detection unit and a set of configuration registers as shown in the subsequent figure.

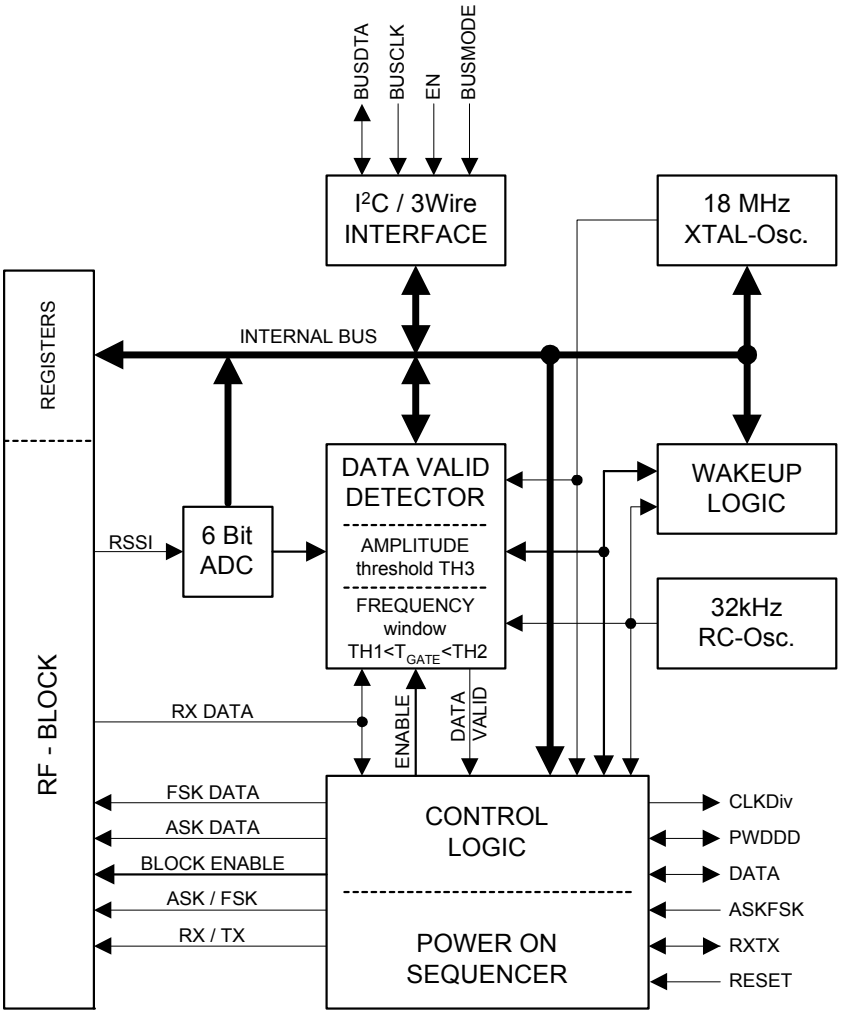


Figure 8 Timing and Data Control Unit

The I²C/3-wire Bus Interface gives an external microcontroller full control over important system parameters at any time.

It is possible to set the device in three different modes: Slave Mode, Self Polling Mode and Timer Mode. This is done by a state machine which is implemented in the WAKEUP LOGIC unit. A detailed description is given in **Chapter 2.4.17**.

The DATA VALID DETECTOR contains a frequency window counter and an RSSI threshold comparator. The window counter uses the incoming data signal from the data slicer as the gating signal and the crystal oscillator frequency as the time base to determine the actual data rate. The result is compared with the expected data rate.

The threshold comparator compares the actual RSSI level with the expected RSSI level.

If both conditions are true the PWDDD pin is set to LOW in self polling mode as you can see in **Chapter 2.4.17**. This signal can be used as an interrupt for an external μP. Because the PWDDD pin is bidirectional and open drain driven by an internal pull-up resistor it is possible to apply an external LOW thus enabling the device.

2.4.15 Bus Interface and Register Definition

The TDA7255V supports the I²C bus protocol (2 wire) and a 3-wire bus protocol. Operation is selectable by the BUSMODE pin (pin 38) as shown in the following table. All bus pins (BUSDTA, BUSCLK, EN, BUSMODE) have a Schmitt-triggered input stage. The BUSDTA pin is bidirectional where the output is open drain driven by an internal 15 kΩ pull up resistor.

Table 6 Bus Interface Format

Function	BUSMODE	EN	BUSCLK	BUSDTA
I²C Mode	Low	High = inactive, Low = active	Clock input	Data in/out
3-wire Mode	High			

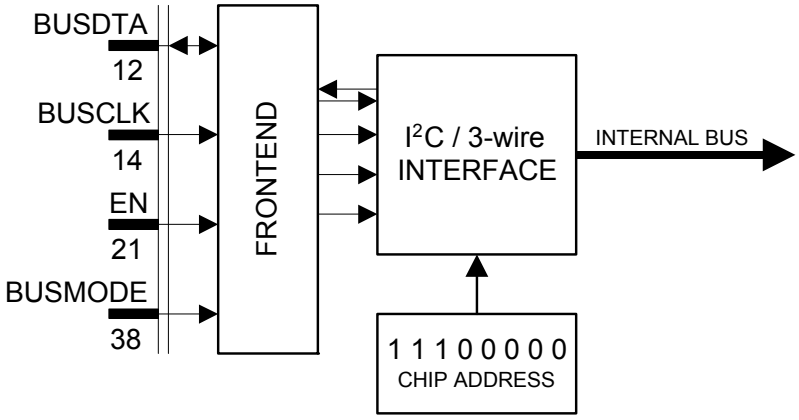


Figure 9 Bus Interface

Note: The interface is able to access the internal registers at any time, even in POWER DOWN mode. There is no internal clock necessary for Interface operation.

2.4.15.1 I²C Bus Mode

In this mode the BUSMODE pin (pin 38) = LOW and the EN pin (pin 21) = LOW.

Data Transition

Data transition on the pin BUSDTA can only occur when BUSCLK is LOW. BUSDTA transitions while BUSCLK is HIGH will be interpreted as start or stop condition.

Start Condition (STA)

A start condition is defined by a HIGH to LOW transition of the BUSDTA line while BUSCLK is HIGH. This start condition must precede any command and initiate a data transfer onto the bus.

Stop Condition (STO)

A stop condition is defined by a LOW to HIGH transition of the BUSDTA line while BUSCLK is HIGH. This condition terminates the communication between the devices and forces the bus interface into the initial state.

Acknowledge (ACK)

Indicates a successful data transfer. The transmitter will release the bus after sending 8 bit of data. During the 9th clock cycle the receiver will set the SDA line to LOW level to indicate it has received the 8 bits of data correctly.

Data Transfer Write Mode

To start the communication, the bus master must initiate a start condition (STA), followed by the 8 bit chip address. The chip address for the TDA7255V is fixed as „1110000“ (MSB at first). The last bit (LSB = A0) of the chip address byte defines the type of operation to be performed:

A0 = 0, a write operation is selected and A0 = 1 a read operation is selected.

After this comparison the TDA7255V will generate an ACK and awaits the desired sub address byte (00H...0FH) and data bytes. At the end of the data transition the master has to generate the stop condition (STO).

Data Transfer Read Mode

To start the communication in the read mode, the bus master must initiate a start condition (STA), followed by the 8 bit chip address (write: A0 = 0), followed by the sub address to read (80H, 81H), followed by the chip address (read: A0 = 1). After that procedure the data of the selected register (80H, 81H) is read out. During this time the data line has to be kept in HIGH state and the chip sends out the data. At the end of data transition the master has to generate the stop condition (STO).

2.4.15.2 Bus Data Format in I²C Mode

Table 7 Chip Address Organization

MSB							LSB	Function
1	1	1	0	0	0	0	0	Chip Address Write
1	1	1	0	0	0	0	1	Chip Address Read

Table 8 I²C Bus Write Mode 8 Bit

	MSB CHIP ADDRESS (WRITE)							LSB		MSB SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH							LSB		MSB DATA IN							LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D7	D6	D5	D4	D3	D2	D1	D0	ACK	STO

Table 9 I²C Bus Write Mode 16 Bit

	MSB CHIP ADDRESS (WRITE)							LSB		MSB SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH, 0FH							LSB		MSB DATA IN							LSB		
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	D15	...	D8	ACK	D7	D6	...	D0	ACK	STO

Table 10 I²C Bus Read Mode

	MSB	CHIP ADDRESS (WRITE)						LSB		MSB	SUB ADDRESS (READ) 80H, 81H						LSB			MSB	CHIP ADDRESS (READ)						LSB	
STA	1	1	1	0	0	0	0	0	ACK	S7	S6	S5	S4	S3	S2	S1	S0	ACK	STA	1	1	1	0	0	0	0	1	ACK

Table 11 I²C Bus Read Mode (continued)

MSB	DATA OUT FROM SUB ADDRESS						LSB		
R7	R6	R5	R4	R3	R2	R1	R0	ACK[1)]	STO

1) Mandatory HIGH

2.4.15.3 3-Wire Bus Mode

In this mode pin 38 (BUSMODE) = HIGH and Pin 12 (BUSDTA) is in the data input/output pin. Pin 21 (EN) is used to activate the bus interface to allow the transfer of data to / from the device. When pin 21 (EN) is inactive (HIGH), data transfer is inhibited.

Data Transition

Data transition on pin 12 (BUSDTA) can only occur if the clock BUSCLK is LOW. To perform a data transfer the interface has to be enabled. This is done by setting the EN line to LOW. A serial transfer is done via BUSDTA, BUSCLK and EN. The bit stream needs no chip address.

Data Transfer Write Mode

To start the communication the EN line has to be set to LOW. The desired sub address byte and data bytes have to follow. The sub-address (00H...0FH) determines which of the data bytes are transmitted. At the end of data transition the EN must be HIGH.

Data Transfer Read Mode

To start the communication in the read mode, the EN line has to be set to LOW followed by the sub address to read (80H, 81H). Afterwards the device is ready to read out data. At the end of data transition EN must be HIGH.

2.4.15.4 Bus Data Format 3-Wire Bus Mode

Table 12 3-Wire Bus Write Mode

MSB	SUB ADDRESS (WRITE) 00H...08H, 0DH, 0EH,0FH						LSB	MSB	DATA IN X...0 (X = 7 or 15)						LSB
S7	S6	S5	S4	S3	S2	S1	S0	DX	...	D5	D4	D3	D2	D1	D0

Table 13 3-Wire Bus Read Mode

MSB	SUB ADDRESS (READ) 80H, 81H						LSB	MSB	DATA OUT FROM SUB ADDRESS						LSB
S7	S6	S5	S4	S3	S2	S1	S0	R7	R6	R5	R4	R3	R2	R1	R0

2.4.15.5 Register Definition

Sub Addresses Overview

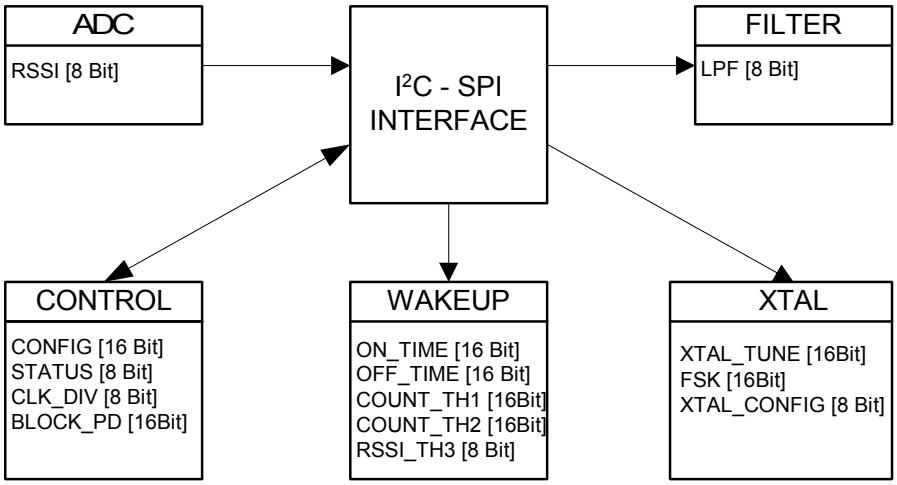


Figure 10 Sub Addresses Overview

Sub Address Organization

Table 14 Sub Addresses of Data Registers Write

MSB							LSB	HEX	Function	Description	Bit Length
0	0	0	0	0	0	0	0	00h	CONFIG	General definition of status bits	16
0	0	0	0	0	0	0	1	01h	FSK	Values for FSK-shift	16
0	0	0	0	0	0	1	0	02h	XTAL_TUNING	Nominal frequency	16
0	0	0	0	0	0	1	1	03h	LPF	I/Q and data filter cutoff frequencies	8
0	0	0	0	0	1	0	0	04h	ON_TIME	ON time of wakeup counter	16
0	0	0	0	0	1	0	1	05h	OFF_TIME	OFF time of wakeup counter	16
0	0	0	0	0	1	1	0	06h	COUNT_TH1	Lower threshold of window counter	16
0	0	0	0	0	1	1	1	07h	COUNT_TH2	Higher threshold of window counter	16
0	0	0	0	1	0	0	0	08h	RSSI_TH3	Threshold for RSSI signal	8
0	0	0	0	1	1	0	1	0Dh	CLK_DIV	Configuration and Ratio of clock divider	8
0	0	0	0	1	1	1	0	0Eh	XTAL_CONFIG	XTAL configuration	8
0	0	0	0	1	1	1	1	0Fh	BLOCK_PD	Building Blocks Power Down	16

Table 15 Sub Addresses of Data Registers Read

MSB							LSB	HEX	Function	Description	Bit Length
1	0	0	0	0	0	0	0	80h	STATUS	Results of comparison: ADC & WINDOW	8
1	0	0	0	0	0	0	1	81h	ADC	ADC data out	8

2.4.16 Registers Chapter

Data Byte Specification

Table 16 Registers Overview

Register Short Name	Register Long Name	Offset Address	Reset Value
Registers Chapter, Register Descriptions			
CONFIG		00_H	$04F9_H$
FSK		01_H	$0A0C_H$
XTAL_TUNING		02_H	0012_H
LPF		03_H	0018_H
ON_TIME		04_H	$FEC0_H$
OFF_TIME		05_H	$F380_H$
COUNT_TH1		06_H	0000_H
COUNT_TH2		07_H	0000_H
RSSI_TH3		08_H	$007F_H$
CLK_DIV		$0D_H$	0008_H
XTAL_CONFIG		$0E_H$	0001_H
BLOCK_PD		$0F_H$	$FFFF_H$
STATUS		80_H	0000_H
ADC		81_H	0000_H

The register is addressed wordwise.

2.4.16.1 Register Descriptions

Data Byte Specification

CONFIG **Offset** 00_H **Reset Value** $04F9_H$

15	14	13	12
SLICER	**ALL_PD**	**TESTMODE**	**CONTROL**
rw	rw	rw	rw
11	10	9	8
ASK_NFSK	**RX_NTX**	**CLK_EN**	**RX_DATA_INV**
rw	rw	rw	rw
7	6	5	4
D_OUT	**ADC_MODE**	**F_COUNT_MODE**	**LNA_GAIN**
rw	rw	rw	rw
3	2	1	0
EN_RX	**MODE_2**	**MODE_1**	**PA_PWR**
rw	rw	rw	rw

Field	Bits	Type	Description
SLICER	15	rw	0_B Lowpass 1_B Peak Detector Reset: 0_B
ALL_PD	14	rw	0_B Normal operation 1_B All Power down Reset: 0_B
TESTMODE	13	rw	0_B Normal operation 1_B Testmode Reset: 0_B
CONTROL	12	rw	0_B RX/TX and ASK/FSK external controlled 1_B Register controlled Reset: 0_B
ASK_NFSK	11	rw	0_B FSK 1_B ASK Reset: 0_B

Field	Bits	Type	Description
RX_NTX	10	rw	0_B TX 1_B RX Reset: 1_B
CLK_EN	9	rw	0_B CLK off during power down 1_B CLK always on, even in power down Reset: 0_B
RX_DATA_INV	8	rw	0_B No Data inversion 1_B Data inversion Reset: 0_B
D_OUT	7	rw	0_B Data out if valid 1_B Always Data out Reset: 1_B
ADC_MODE	6	rw	0_B One shot 1_B Continuous Reset: 1_B
F_COUNT_MODE	5	rw	0_B One shot 1_B Continuous Reset: 1_B
LNA_GAIN	4	rw	0_B Low gain 1_B High gain Reset: 1_B
EN_RX	3	rw	0_B Disable receiver 1_B Enable receiver (in self polling and timer mode)[1)] Reset: 1_B
MODE_2	2	rw	0_B Slave mode 1_B Timer mode Reset: 0_B
MODE_1	1	rw	0_B Slave or timer mode 1_B Self polling mode Reset: 0_B
PA_PWR	0	rw	0_B Low TX Power 1_B High TX Power Reset: 1_B

1) Function is only active in self-polling and timer mode. When D3 is set to LOW the RX path is not enabled if PWDDD pin is set to LOW. A delayed setting of D3 results in a delayed power ON of the RX building blocks.

FSK

FSK **Offset** **Reset Value**

01_H **$0A0C_H$**

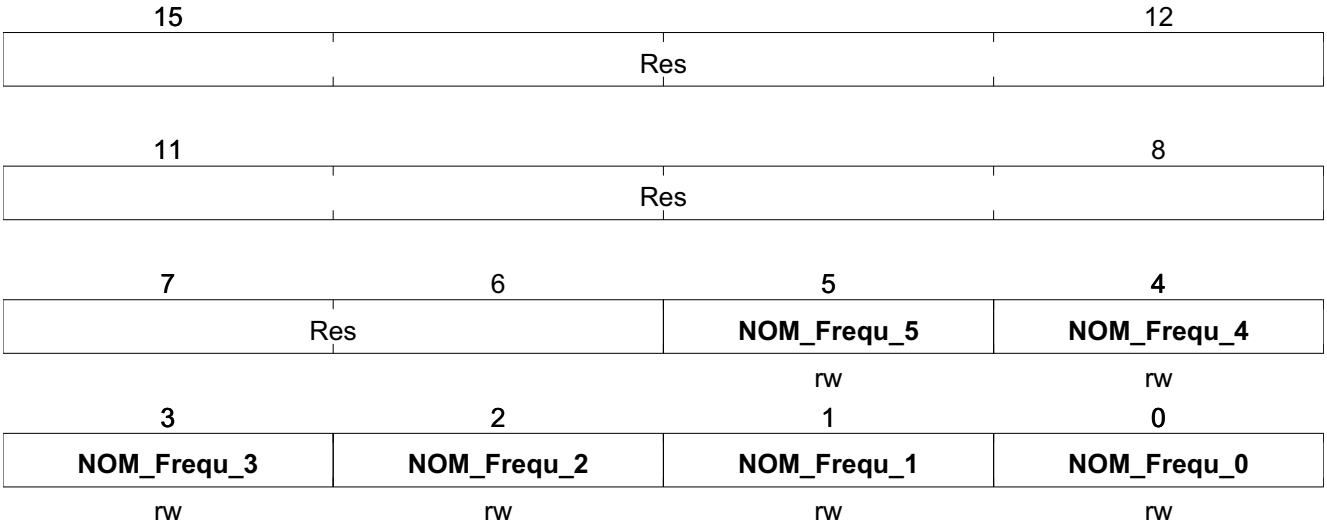
15	14	13	12
Res		**FSK_High_5**	**FSK_High_4**
		rw	rw
11	**10**	**9**	**8**
FSK_High_3	**FSK_High_2**	**FSK_High_1**	**FSK_High_0**
rw	rw	rw	rw
7	**6**	**5**	**4**
Res		**FSK_Low_5**	**FSK_Low_4**
		rw	rw
3	**2**	**1**	**0**
FSK_Low_3	**FSK_Low_2**	**FSK_Low_1**	**FSK_Low_0**
rw	rw	rw	rw

Field	Bits	Type	Description
FSK_High_5	13	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 8 pF Reset: 0_B
FSK_High_4	12	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 4 pF Reset: 0_B
FSK_High_3	11	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 2 pF Reset: 1_B
FSK_High_2	10	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 1 pF Reset: 0_B
FSK_High_1	9	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 500 fF Reset: 1_B
FSK_High_0	8	rw	**Setting for positive frequency shift: FSK_High or ASK-RX** 1_B 250 fF Reset: 0_B
FSK_Low_5	5	rw	**Setting for negative frequency shift: FSK_Low** 1_B 4 pF Reset: 0_B

Field	Bits	Type	Description
FSK_Low_4	4	rw	**Setting for negative frequency shift: FSK_Low** 1_B 2 pF Reset: 0_B
FSK_Low_3	3	rw	**Setting for negative frequency shift: FSK_Low** 1_B 1 pF Reset: 1_B
FSK_Low_2	2	rw	**Setting for negative frequency shift: FSK_Low** 1_B 500 fF Reset: 1_B
FSK_Low_1	1	rw	**Setting for negative frequency shift: FSK_Low** 1_B 250 fF Reset: 0_B
FSK_Low_0	0	rw	**Setting for negative frequency shift: FSK_Low** 1_B 125 fF Reset: 0_B

XTAL_TUNING

XTAL_TUNING **Offset** 02_H **Reset Value** 0012_H



Field	Bits	Type	Description
NOM_Frequ_5	5	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 8 pF Reset: 0_B
NOM_Frequ_4	4	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 4 pF Reset: 1_B
NOM_Frequ_3	3	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 2 pF Reset: 0_B
NOM_Frequ_2	2	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 1 pF Reset: 0_B
NOM_Frequ_1	1	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 500 fF Reset: 1_B
NOM_Frequ_0	0	rw	**Setting for nominal frequency ASK-TX, FSK-RX** 1_B 250 fF Reset: 0_B

LPF

LPF | **Offset** 03_H | **Reset Value** 0018_H

15			12
Res			

11			8
Res			

7	6	5	4
Datafilter_3	**Datafilter_2**	**Datafilter_1**	**Datafilter_0**
rw	rw	rw	rw

3	2	1	0
Q_Filter_2	**Q_Filter_1**	**Q_Filter_0**	Res
rw	rw	rw	

Field	Bits	Type	Description
Datafilter_3	7	rw	**3 dB cutoff frequency of data filter** Reset: 0_B
Datafilter_2	6	rw	**3 dB cutoff frequency of data filter** Reset: 0_B
Datafilter_1	5	rw	**3 dB cutoff frequency of data filter** Reset: 0_B
Datafilter_0	4	rw	**3 dB cutoff frequency of data filter** Reset: 1_B
Q_Filter_2	3	rw	**3 dB cutoff frequency of IQ-filter** Reset: 1_B
Q_Filter_1	2	rw	**3 dB cutoff frequency of IQ-filter** Reset: 0_B
Q_Filter_0	1	rw	**3 dB cutoff frequency of IQ-filter** Reset: 0_B

ON_TIME

ON_TIME	Offset	Reset Value
	04_H	$FEC0_H$

15	14	13	12
ON_15	**ON_14**	**ON_13**	**ON_12**
rw	rw	rw	rw
11	10	9	8
ON_11	**ON_10**	**ON_9**	**ON_8**
rw	rw	rw	rw
7	6	5	4
ON_7	**ON_6**	**ON_5**	**ON_4**
rw	rw	rw	rw
3	2	1	0
ON_3	**ON_2**	**ON_1**	**ON_0**
rw	rw	rw	rw

Field	Bits	Type	Description
ON_15	15	rw	Reset: 1_B
ON_14	14	rw	Reset: 1_B
ON_13	13	rw	Reset: 1_B
ON_12	12	rw	Reset: 1_B
ON_11	11	rw	Reset: 1_B
ON_10	10	rw	Reset: 1_B
ON_9	9	rw	Reset: 1_B
ON_8	8	rw	Reset: 0_B
ON_7	7	rw	Reset: 1_B
ON_6	6	rw	Reset: 1_B
ON_5	5	rw	Reset: 0_B

Field	Bits	Type	Description
ON_4	4	rw	Reset: 0_B
ON_3	3	rw	Reset: 0_B
ON_2	2	rw	Reset: 0_B
ON_1	1	rw	Reset: 0_B
ON_0	0	rw	Reset: 0_B

OFF_TIME

OFF_TIME | **Offset** 05_H | **Reset Value** $F380_H$

15	14	13	12
OFF_15	**OFF_14**	**OFF_13**	**OFF_12**
rw	rw	rw	rw
11	10	9	8
OFF_11	**OFF_10**	**OFF_9**	**OFF_8**
rw	rw	rw	rw
7	6	5	4
OFF_7	**OFF_6**	**OFF_5**	**OFF_4**
rw	rw	rw	rw
3	2	1	0
OFF_3	**OFF_2**	**OFF_1**	**OFF_0**
rw	rw	rw	rw

Field	Bits	Type	Description
OFF_15	15	rw	Reset: 1_B
OFF_14	14	rw	Reset: 1_B
OFF_13	13	rw	Reset: 1_B
OFF_12	12	rw	Reset: 1_B
OFF_11	11	rw	Reset: 0_B
OFF_10	10	rw	Reset: 0_B
OFF_9	9	rw	Reset: 1_B
OFF_8	8	rw	Reset: 1_B
OFF_7	7	rw	Reset: 1_B
OFF_6	6	rw	Reset: 0_B
OFF_5	5	rw	Reset: 0_B

Field	Bits	Type	Description
OFF_4	4	rw	Reset: 0_B
OFF_3	3	rw	Reset: 0_B
OFF_2	2	rw	Reset: 0_B
OFF_1	1	rw	Reset: 0_B
OFF_0	0	rw	Reset: 0_B

COUNT_TH1

COUNT_TH1 | **Offset** 06_H | **Reset Value** 0000_H

15			12
Res			

11	10	9	8
TH1_11	**TH1_10**	**TH1_9**	**TH1_8**
rw	rw	rw	rw
7	6	5	4
TH1_7	**TH1_6**	**TH1_5**	**TH1_4**
rw	rw	rw	rw
3	2	1	0
TH1_3	**TH1_2**	**TH1_1**	**TH1_0**
rw	rw	rw	rw

Field	Bits	Type	Description
TH1_11	11	rw	Reset: 0_B
TH1_10	10	rw	Reset: 0_B
TH1_9	9	rw	Reset: 0_B
TH1_8	8	rw	Reset: 0_B
TH1_7	7	rw	Reset: 0_B
TH1_6	6	rw	Reset: 0_B
TH1_5	5	rw	Reset: 0_B
TH1_4	4	rw	Reset: 0_B
TH1_3	3	rw	Reset: 0_B
TH1_2	2	rw	Reset: 0_B
TH1_1	1	rw	Reset: 0_B

Field	Bits	Type	Description
TH1_0	0	rw	Reset: 0_B

COUNT_TH2

COUNT_TH2 | **Offset** 07_H | **Reset Value** 0000_H

15			12
Res			

11	10	9	8
TH2_11	**TH2_10**	**TH2_9**	**TH2_8**
rw	rw	rw	rw
7	**6**	**5**	**4**
TH2_7	**TH2_6**	**TH2_5**	**TH2_4**
rw	rw	rw	rw
3	**2**	**1**	**0**
TH2_3	**TH2_2**	**TH2_1**	**TH2_0**
rw	rw	rw	rw

Field	Bits	Type	Description
TH2_11	11	rw	Reset: 0_B
TH2_10	10	rw	Reset: 0_B
TH2_9	9	rw	Reset: 0_B
TH2_8	8	rw	Reset: 0_B
TH2_7	7	rw	Reset: 0_B
TH2_6	6	rw	Reset: 0_B
TH2_5	5	rw	Reset: 0_B
TH2_4	4	rw	Reset: 0_B
TH2_3	3	rw	Reset: 0_B
TH2_2	2	rw	Reset: 0_B
TH2_1	1	rw	Reset: 0_B

Field	Bits	Type	Description
TH2_0	0	rw	Reset: 0_B

RSSI_TH3

RSSI_TH3 | **Offset** 08_H | **Reset Value** $007F_H$

15	14	13	12
Res			

11	10	9	8
Res			

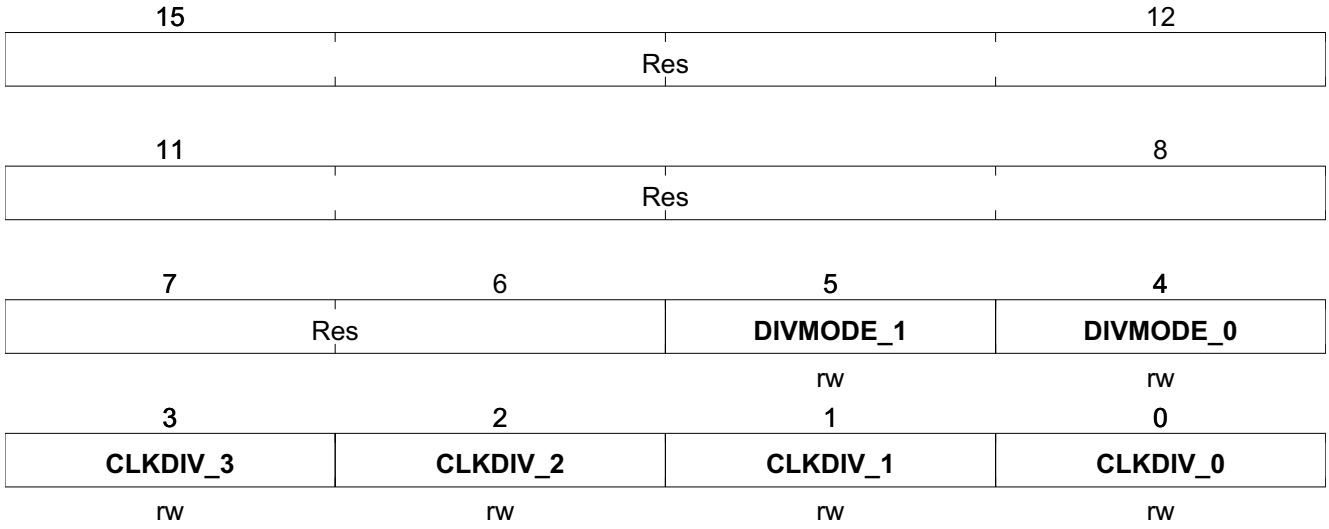
7	6	5	4
Res	**SELECT**	**TH3_5**	**TH3_4**
	rw	rw	rw

3	2	1	0
TH3_3	**TH3_2**	**TH3_1**	**TH3_0**
rw	rw	rw	rw

Field	Bits	Type	Description
SELECT	6	rw	0_B VCC 1_B RSSI Reset: 1_B
TH3_5	5	rw	Reset: 1_B
TH3_4	4	rw	Reset: 1_B
TH3_3	3	rw	Reset: 1_B
TH3_2	2	rw	Reset: 1_B
TH3_1	1	rw	Reset: 1_B
TH3_0	0	rw	Reset: 1_B

CLK_DIV

CLK_DIV | **Offset** $0D_H$ | **Reset Value** 0008_H



Field	Bits	Type	Description
DIVMODE_1	5	rw	Reset: 0_B
DIVMODE_0	4	rw	Reset: 0_B
CLKDIV_3	3	rw	Reset: 1_B
CLKDIV_2	2	rw	Reset: 0_B
CLKDIV_1	1	rw	Reset: 0_B
CLKDIV_0	0	rw	Reset: 0_B

XTAL_CONFIG

XTAL_CONFIG | **Offset** $0E_H$ | **Reset Value** 0001_H

15			12
Res			
11			**8**
Res			
7			**4**
Res			

3	2	1	0
Res	**FSK_Ramp_0**	**FSK_Ramp_1**	**Bipolar_FET**
	rw	rw	rw

Field	Bits	Type	Description
FSK_Ramp_0	2	rw	**Only in bipolar mode** Reset: 0_B
FSK_Ramp_1	1	rw	**Only in bipolar mode** Reset: 0_B
Bipolar_FET	0	rw	0_B FET 1_B Bipolar Reset: 1_B

BLOCK_PD

BLOCK_PD — **Offset** $0F_H$ — **Reset Value** $FFFF_H$

15	14	13	12
REF_PD	**RC_PD**	**WINDOW_PD**	**ADC_PD**
rw	rw	rw	rw
11	10	9	8
PEAK_DET_PD	**DATA_SLIC_PD**	**DATA_FIL_PD**	**QUAD_PD**
rw	rw	rw	rw
7	6	5	4
LIM_PD	**I/Q_FIL_PD**	**MIX2_PD**	**MIX1_PD**
rw	rw	rw	rw
3	2	1	0
LNA_PD	**PA_PD**	**PLL_PD**	**XTAL_PD**
rw	rw	rw	rw

Field	Bits	Type	Description
REF_PD	15	rw	1_B Power down Band Gap Reference Reset: 1_B
RC_PD	14	rw	1_B Power down RC Oscillator Reset: 1_B
WINDOW_PD	13	rw	1_B Power down Window Counter Reset: 1_B
ADC_PD	12	rw	1_B Power down ADC Reset: 1_B
PEAK_DET_PD	11	rw	1_B Power down Peak Detectors Reset: 1_B
DATA_SLIC_PD	10	rw	1_B Power down Data Slicer Reset: 1_B
DATA_FIL_PD	9	rw	1_B Power down Data Filter Reset: 1_B

Field	Bits	Type	Description
QUAD_PD	8	rw	1_B Power down Quadri Correlator Reset: 1_B
LIM_PD	7	rw	1_B Power down Limiter Reset: 1_B
I/Q_FIL_PD	6	rw	1_B Power down I/Q Filters Reset: 1_B
MIX2_PD	5	rw	1_B Power down I/Q Mixer Reset: 1_B
MIX1_PD	4	rw	1_B Power down 1st Mixer Reset: 1_B
LNA_PD	3	rw	1_B Power down LNA Reset: 1_B
PA_PD	2	rw	1_B Power down Power Amplifier Reset: 1_B
PLL_PD	1	rw	1_B Power down PLL Reset: 1_B
XTAL_PD	0	rw	1_B Power down XTAL Oscillator Reset: 1_B

STATUS

STATUS | **Offset** 80_H | **Reset Value** 0000_H

15	14	13	12
Res			

11	10	9	8
Res			

7	6	5	4
COMP_LOW	**COMP_IN**	**COMP_HIGH**	**COMP_05_LOW**
rw	rw	rw	rw
3	2	1	0
COMP_05_IN	**COMP_05_HIGH**	**RSSI_TH3**	**RSSI_TH3**
rw	rw	rw	rw

Field	Bits	Type	Description
COMP_LOW	7	rw	1_B If data rate < TH1
COMP_IN	6	rw	1_B If TH1 < data rate < TH2
COMP_HIGH	5	rw	1_B If TH2 < data rate
COMP_05_LOW	4	rw	1_B If data rate < 0,5*TH1
COMP_05_IN	3	rw	1_B If 0,5*TH1 < data rate < 0,5*TH2
COMP_05_HIGH	2	rw	1_B If 0,5*TH2 < data rate
RSSI_TH3	1	rw	1_B If RSSI value is equal TH3
RSSI_TH3	0	rw	1_B If RSSI value is greater than TH3

ADC

ADC **Offset** **Reset Value**

81_H **0000_H**

15			12
Res			

11			8
Res			

7	6	5	4
PD_ADC	**SELECT**	**RSSI_5**	**RSSI_4**
rw	rw	rw	rw
3	2	1	0
RSSI_3	**RSSI_2**	**RSSI_1**	**RSSI_0**
rw	rw	rw	rw

Field	Bits	Type	Description
PD_ADC	7	rw	ADC power down feedback Bit
SELECT	6	rw	SELECT feedback Bit
RSSI_5	5	rw	RSSI value Bit5
RSSI_4	4	rw	RSSI value Bit4
RSSI_3	3	rw	RSSI value Bit3
RSSI_2	2	rw	RSSI value Bit2
RSSI_1	1	rw	RSSI value Bit1
RSSI_0	0	rw	RSSI value Bit0

2.4.17 Wakeup Logic

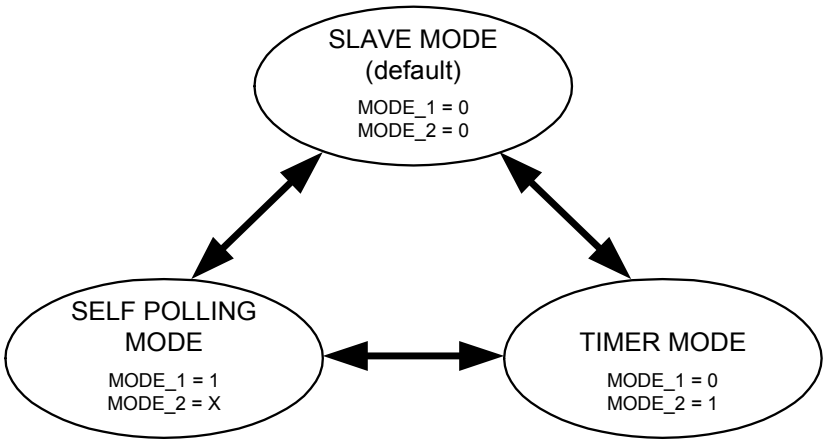


Figure 11 Wakeup Logic States

Table 17 MODE Settings: CONFIG Register

MODE_1	MODE_2	MODE
0	0	SLAVE MODE
0	1	TIMER MODE
1	X	SELF POLLING MODE

SLAVE MODE

The receive and transmit operation is fully controlled by an external control device via the respective RXTX, ASKFSK, PWDDD, and DATA pins. The wakeup logic is inactive in this case.

After RESET or 1st Power-up the chip is in SLAVE MODE. By setting MODE_1 and MODE_2 in the CONFIG register the mode may be changed.

SELF POLLING MODE

The chip turns itself on periodically to receive using a built-in 32 kHz RC oscillator. The timing of this is determined by the ON_TIME and OFF_TIME registers, the duty cycle can be set between 0 and 100% in 31.25 µs increments. The data detect logic is enabled and a 15 µs LOW impulse is provided at PWDDD pin (Pin 24), if the received data is valid.

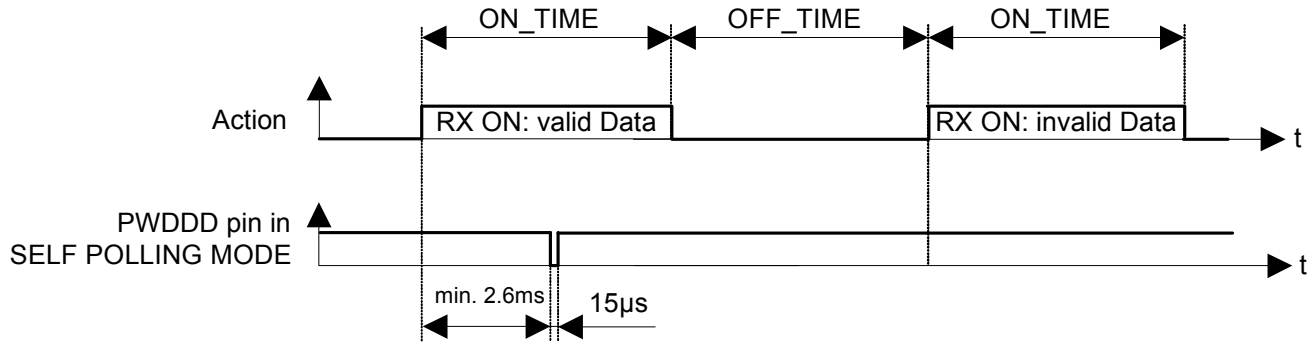


Figure 12 Timing for Self Polling Mode (ADC & Data detect in One Shot Mode)

Note: The time delay between start of ON_TIME and the 15 µs LOW impulse is 2.6 ms + 3 period of data rate.

If ADC & Data Detect Logic are in continuous mode the 15 µs LOW impulse is applied at PWDDD after each data valid decision.

In self polling mode if D9 = 0 (Register 00h) and when PWDDD pin level is HIGH the CLK output is on during ON_TIME and off during OFF_TIME. If D9 = 1, the CLK output is always on.

TIMER MODE

Only the internal Timer (determined by the ON_TIME and OFF_TIME registers) is active to support an external logic with periodical Interrupts. After ON_TIME + OFF_TIME a 15 µs LOW impulse is applied at the PWDDD pin (Pin 24).

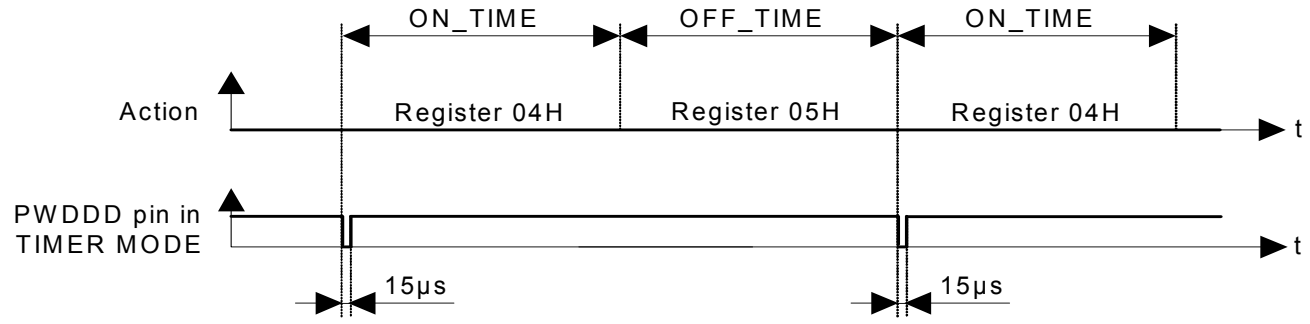


Figure 13 Timing for Timer Mode

Please note to add a serial resistor in the V_{DD} supply line as mentioned on page 13 and in **Chapter 4.4**

2.4.18 Data Valid Detection, Data Pin

Data signals generate a typical spectrum and this can be used to determine if valid data is on air.

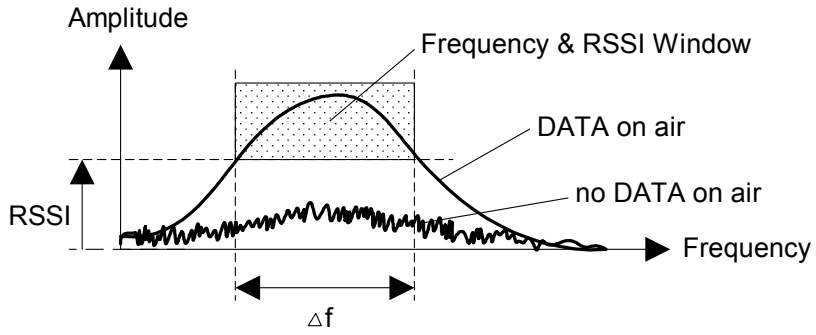


Figure 14 Frequency and RSSI Window

The “data valid” criterion is generated from the result of RSSI-TH3 comparison and t_{GATE} between TH1 and TH2 result as shown below. In case of Manchester coding the 0,5*TH1 and 0,5*TH2 gives improved performance.

The use of permanent data valid recognition makes it absolutely necessary to set the RSSI-ADC and the Window counter into continuous mode (Register 00H, Bit D5 = D6 = 1).

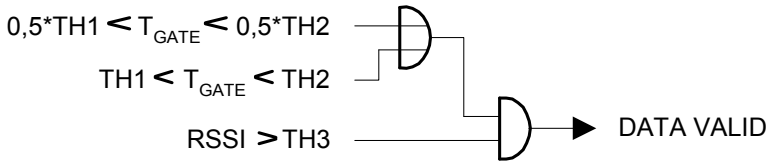


Figure 15 Data Valid Circuit

D_OUT and RX_DATA_INV from the CONFIG register determine the output of DATA at Pin 25. RXTXint and TX_ON are internally generated signals.

In RX and power down mode DATA pin (Pin 25) is tied to GND.

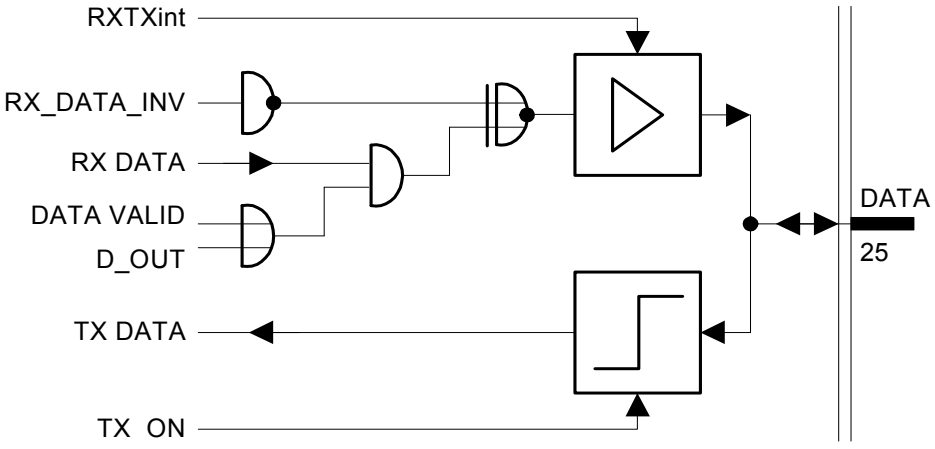


Figure 16 Data Input / Output Circuit

2.4.19 Sequence Timer

The sequence timer has to control all the enable signals of the analog components inside the chip. The time base is the 32 kHz RC oscillator.

After the first POWER ON or RESET a 1 MHz clock is available at the clock output pin. This clock output can be used by an external µC to set the system into the desired state and outputs valid data after 500 μs (see **Figure 17** and **Figure 18**, t_{CLKSU})

There are two possibilities to start the device after a reset or first power on:

- PWDDD pin is LOW: Normal operation timing is performed after t_{SYSSU} (see **Figure 17**).
- PWDDD pin is HIGH (device in power down mode): A clock is offered at the clock output pin until the device is activated (PWDDD pin is pulled to LOW). After the first activation the time t_{SYSSU} is required until normal operation timing is performed (see **Figure 18**).
  This could be used to extend the clock generation without device programming or activation.

Note: It is required to activate the device for the duration of t_{SYSSU} after first power on or a reset. Only if this is done the normal operation timing is performed.

With default settings the clock generating units are disabled during PD, therefore no clock is available at the clock output pin. It is possible to offer a clock signal at the clock output pin every time (also during PD) if the CLK_EN Bit in the CONFIG register is set to HIGH.

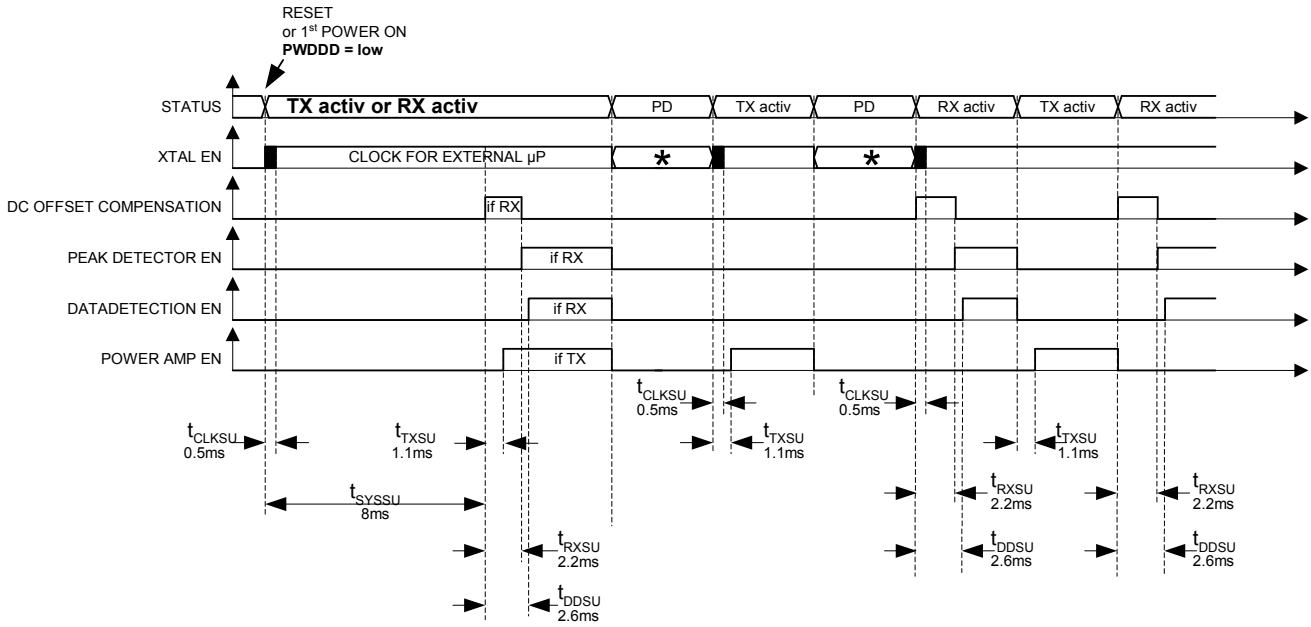


Figure 17 1st Start or Reset in Active Mode

Note: The time values are typical values

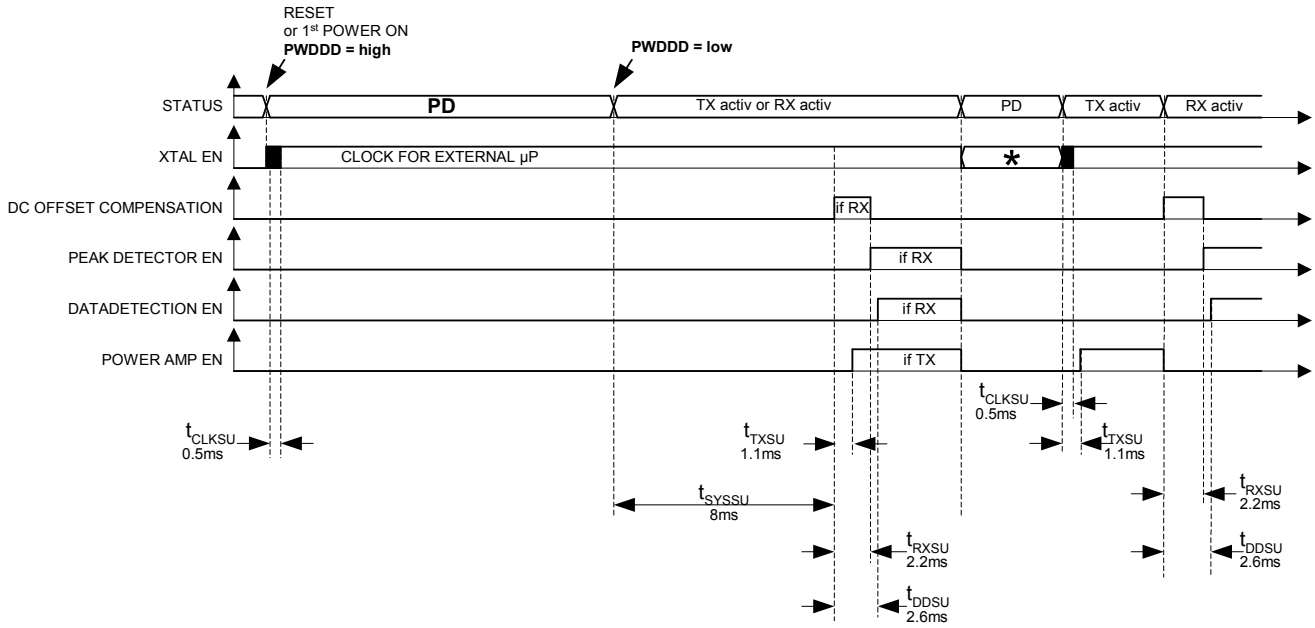


Figure 18 1st Start or Reset in PD Mode

***** State is either „I“ or „O“ depending on time of setting into powerdown

Note: The time values are typical values

This means that the device needs t_{DDSU} setup time to start the data detection after RX is activated. When activating TX it requires t_{TXSU} setup time to enable the power amplifier.

For timing information refer to **Chapter 4.3**.

For test purposes a TESTMODE is provided by the Sequencer as well. In this mode the BLOCK_PD register be set to various values. This will override the Sequencer timing. Depending on the settings in Config Register 00H the corresponding building blocks are enabled, as shown in the subsequent figure.

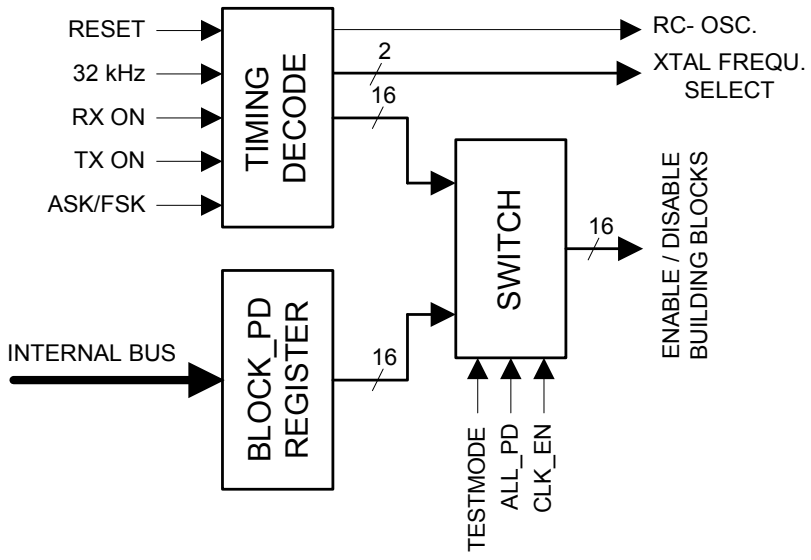


Figure 19 Sequencer‘s Capability

2.4.20 Clock Divider

It supports an external logic with a programmable Clock at pin 23 (CLKDIV).

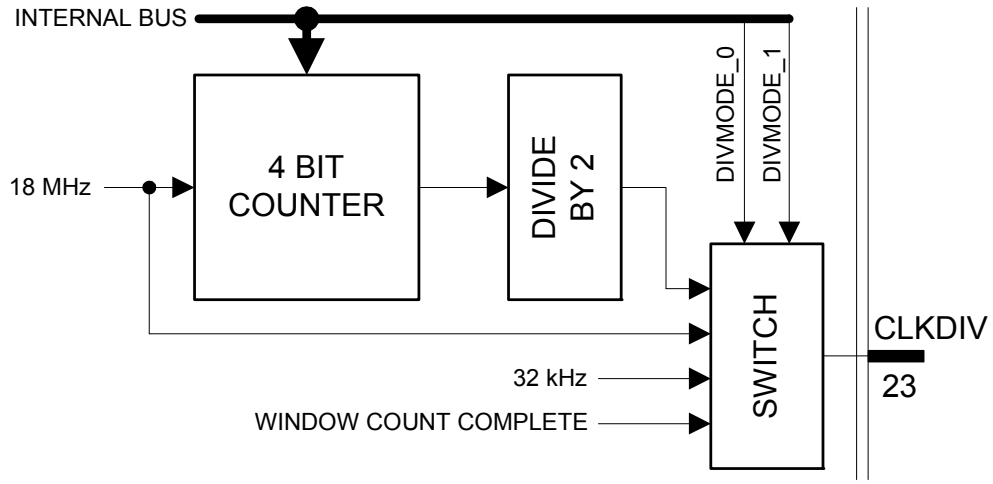


Figure 20 Clock Divider

The Output Selection and Divider Ratio can be set in the CLK_DIV register.

Table 18 CLK_DIV Output Selection

D5	D4	Output
0	0	Output from Divider (default)
0	1	18.089 MHz
1	0	32 kHz
1	1	Window Count Complete

*Note: Data are valid 500 µs after the crystal oscillator is enabled (see **Figure 17** and **Figure 18**, t_{CLKSU}).*

Table 19 CLK_DIV Setting

D3	D2	D1	D0	Total Divider Ratio	Output Frequency [MHz]
0	0	0	0	2	9,0
0	0	0	1	4	4,5
0	0	1	0	6	3,0
0	0	1	1	8	2,25
0	1	0	0	10	1,80
0	1	0	1	12	1,50
0	1	1	0	14	1,28
0	1	1	1	16	1,125
1	0	0	0	18	1,00 (default)
1	0	0	1	20	0,90
1	0	1	0	22	0,82
1	0	1	1	24	0,75

Table 19 CLK_DIV Setting (cont'd)

D3	D2	D1	D0	Total Divider Ratio	Output Frequency [MHz]
1	1	0	0	26	0,69
1	1	0	1	28	0,64
1	1	1	0	30	0,60
1	1	1	1	32	0,56

Note: As long as default settings are used, there is no clock available at the clock output during Power Down. It is possible to enable the clock during Power Down by setting CLK_EN (Bit D9) in the Config Register (00H) to HIGH.

2.4.21 RSSI and Supply Voltage Measurement

The input of the 6 Bit-ADC can be switched between two different sources: the RSSI voltage (default setting) or a resistor network dividing the V_{cc} voltage by 5.

Table 20 Source for 6 Bit-ADC Selection (Register 08H)

SELECT	Input for 6 Bit-ADC
0	V_{cc} / 5
1	RSSI (default)

To prevent wrong interpretation of the ADC information (read from Register 81H: ADC) you can use the ADC-Power Down feedback Bit (D7) and the SELECT feedback Bit (D6) which correspond to the actual measurement.

*Note: As shown in **Chapter 2.4.19** there is a setup time of 2.6 ms after RX activating. Thus the measurement of RSSI voltage does only make sense after this setup time.*

3 Application

3.1 LNA and PA Matching

3.1.1 RX/TX-Switch

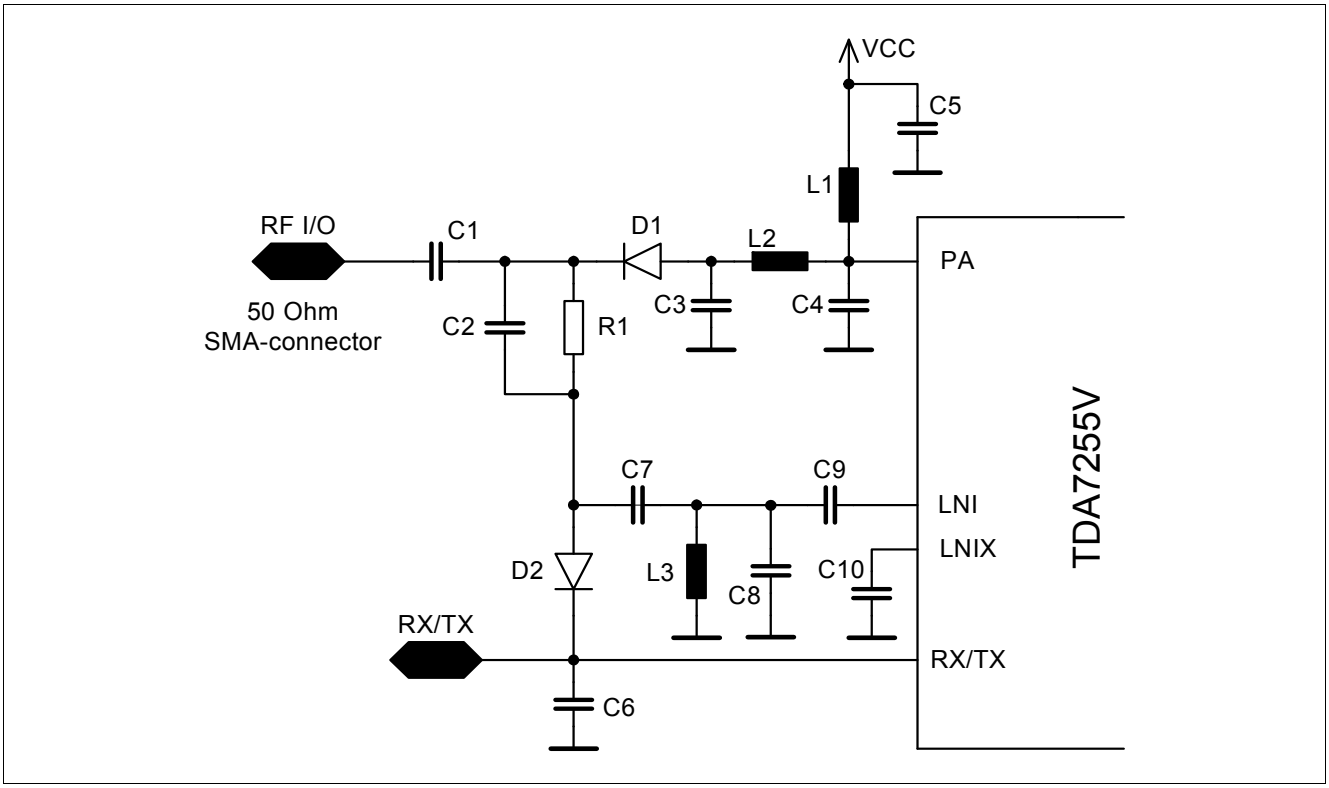


Figure 21 RX/TX-Switch

The RX/TX-switch combines the PA-output and the LNA-input into a single 50 Ω SMA-connector. Two pin-diodes are used as switching elements. If no current flows through a pin diode, it works as a high impedance for RF with very low capacitance. If the pin-diode is forward biased, it provides a low impedance path for RF. (some Ohm)

3.1.2 Switch in RX-Mode

The RX/TX-switch is set to the receive mode by either applying a high level or an open to the RX/TX-jumper on the evaluation-board or by leaving it open. Then both pin-diodes are not biased and therefore have a high impedance.

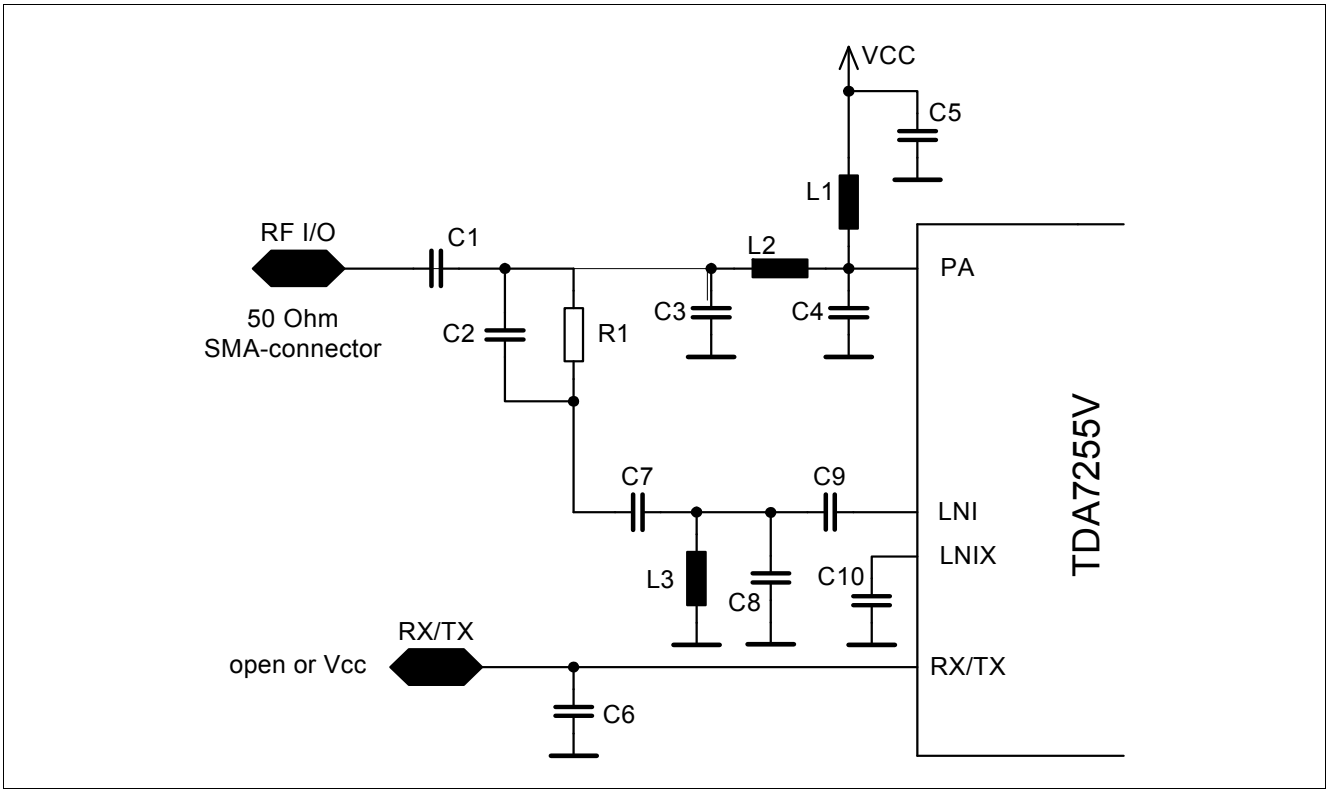


Figure 22 RX-Mode

The RF-signal is able to run from the RF-input-SMA-connector to the LNA-input-pin LNI via C1, C2, C7, L3 and C9. R1 does not affect the matching circuit due to its high resistance. The other input of the differential LNA LNIX can always be AC-grounded using a large capacitor without any loss of performance. In this case the differential LNA can be used as a single ended LNA, which is easier to match. The S11 of the LNA at pin LNI on the evalboard is 0.958/-20° (equals a resistor of 2.26 kΩ in parallel to a capacitor of 1.29 pF) for both high and low-gain-mode of the LNA. (pin LNIX AC-grounded) This impedance has to be matched to 50 Ω with the parts C9, L3, C7 and C2. C1 is a DC-decoupling-capacitor. On the evalboard the most important matching components are (shunt) L3 and (series) C7, C2. The capacitors is mainly a DC-decoupling-capacitor and may be used for some fine tuning of the matching circuit. A good CAE tool (featuring smith-chart) may be used for the calculation of the values of the components. However, the final values of the matching components always have to be found on the board because of the parasitics of the board, which highly influence the matching circuit at RF.

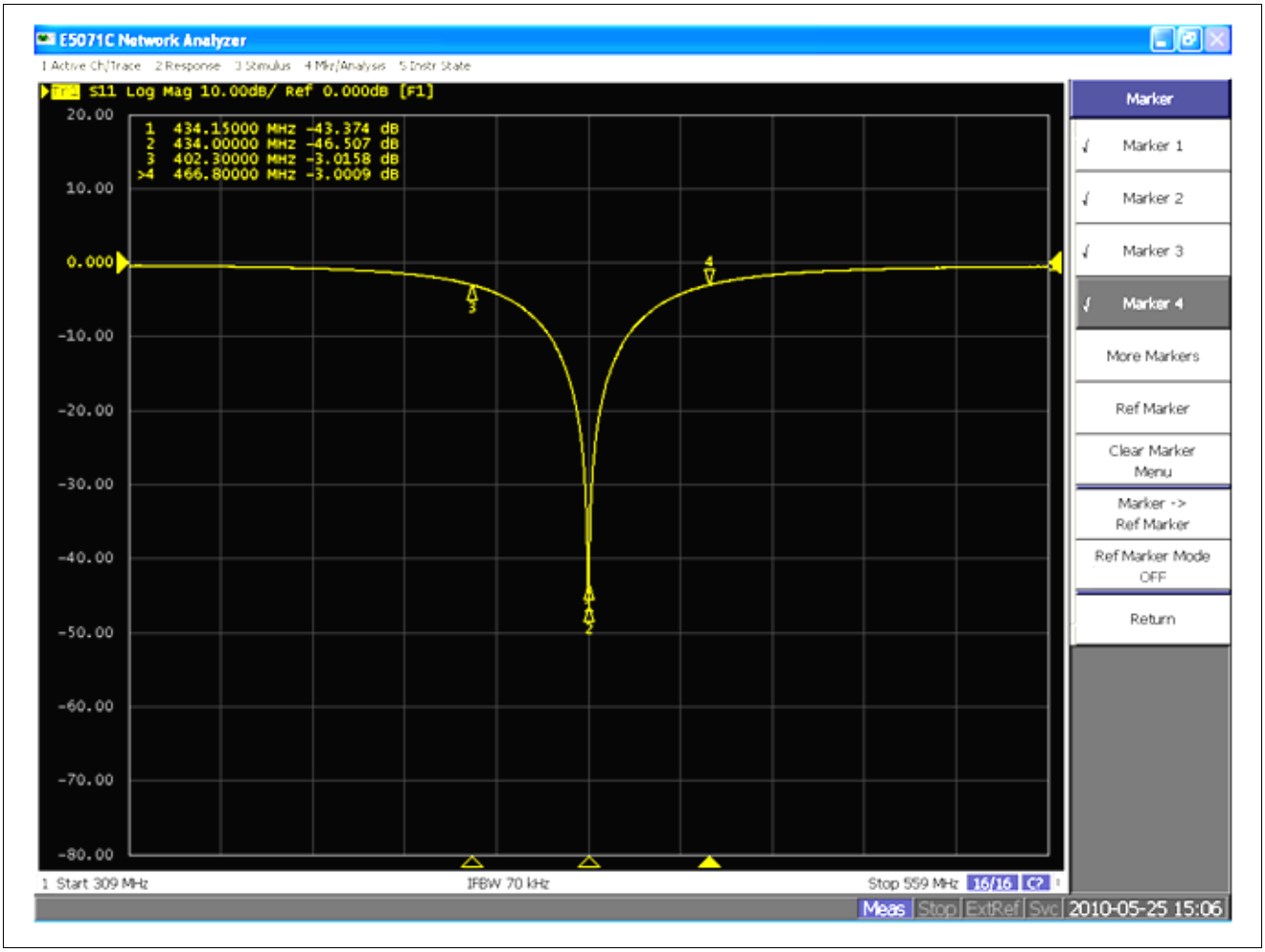


Figure 23 S11 Measured

Above you can see the measured S11 of the evalboard. The –3 dB-points are at 402.3 MHz and 466.8 MHz. So the 3 dB-bandwidth is:

$$B = f_U - f_L = 466.8MHz - 402.3MHz = 64.5MHz \tag{2}$$

$$Q_L = \frac{f_{center}}{B} = \frac{434{,}15MHz}{64{,}5MHz} = 6{,}73 \tag{3}$$

The unloaded Q of the resonant circuit is equal to the Q of the inductor due to its losses.

$$Q_U = Q_{INDUCTOR} \approx 40 @ 434MHz \tag{4}$$

An approximation of the losses of the input matching network can be made with the formula:

$$Loss = -20 \cdot \log\left[1 - \frac{Q_L}{Q_U}\right] = -20 \cdot \log\left[1 - \frac{6{,}73}{40}\right] = 1{,}6dB \tag{5}$$

The noise figure of the LNA-input-matching network is equal to its losses. The input matching network is always a compromise of sensitivity and selectivity. The loaded Q should not get too high because of two reasons:

- More losses in the matching network and hence less sensitivity
- Tolerances of components affect matching too much. This will cause problems in a tuning-free mass production of the application. A good CAE-tool will help to see the effects of component tolerances on the input matching more accurate by tweaking each value.

A very high selectivity can be reached by using SAW-filters at the expense of higher cost and lower sensitivity which will be reduced by the losses of the SAW-filter of approx. 4 dB.

Image-Suppression

Due to the quite high 1st-IF of the frontend, the image frequency is quite far away. The image frequency of the receiver is at:

$$f_{IMAGE} = f_{SIGNAL} + 2 \cdot f_{IF} = 434{,}15MHz + 2 \cdot 144{,}72 = 723{,}59MHz \quad (6)$$

The image suppression on the evalboard is about tbd.dB.

LO-Leakage

The LO of the 1st Mixer is at:

$$f_{LO} = f_{RECEIVE} \cdot \frac{4}{3} = 434{,}15MHz \cdot \frac{4}{3} = 578{,}86MHz \quad (7)$$

The LO-leakage of the evalboard on the RF-input is about –108 dBm. This is far below the ETSI-radio-regulation-limit for LO-leakage.

3.1.3 Switch in TX-Mode

The evalboard can be set into the TX-Mode by grounding the RX/TX-jumper on the evalboard or programming the TDA7255V to operate in the TX-Mode. If the IC is programmed to operate in the TX-Mode, the RX/TX-pin will act as an open drain output at a logical LOW. Then a DC-current can flow from VCC to GND via L1, L2, D1, R1 and D2.

$$P_{PIN-DIODE} = \frac{V_{CC} - 2 \cdot V_{FORWARD,PIN-DIODE}}{R_1} \quad (8)$$

Now both pin-diodes are biased with a current of approx. 0.3 mA @ 3 V and have a very low impedance for RF.

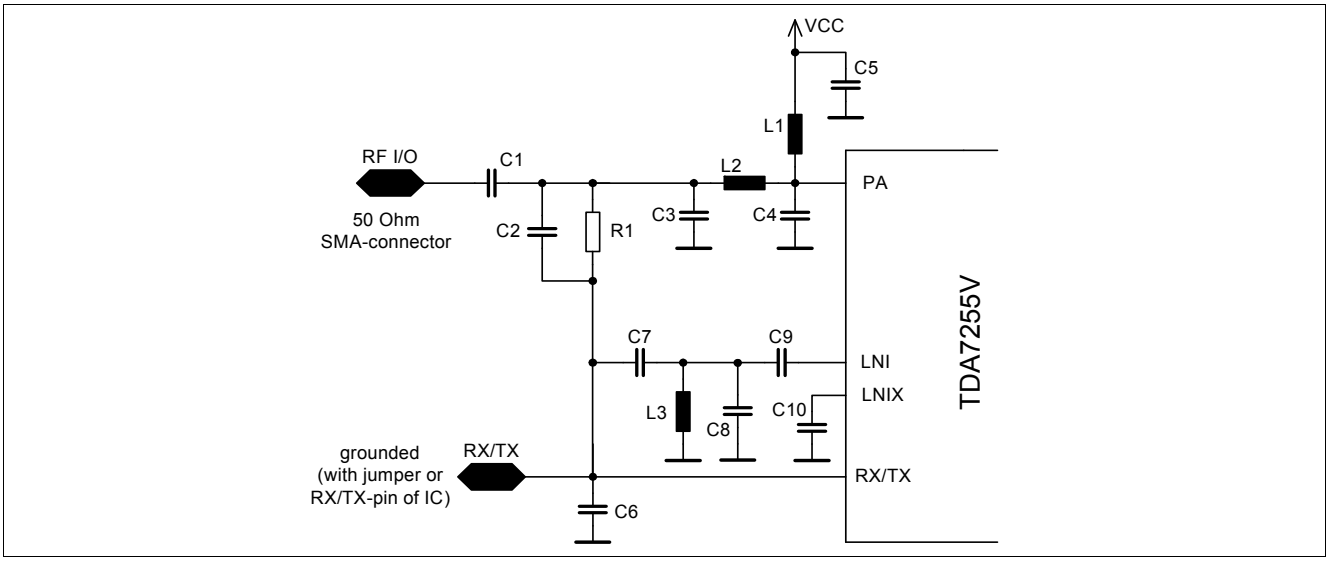


Figure 24 TX_Mode

R1 does not influence the matching because of its very high resistance. Due to the large capacitance of C1, C6 and C5 the circuit can be further simplified for RF:

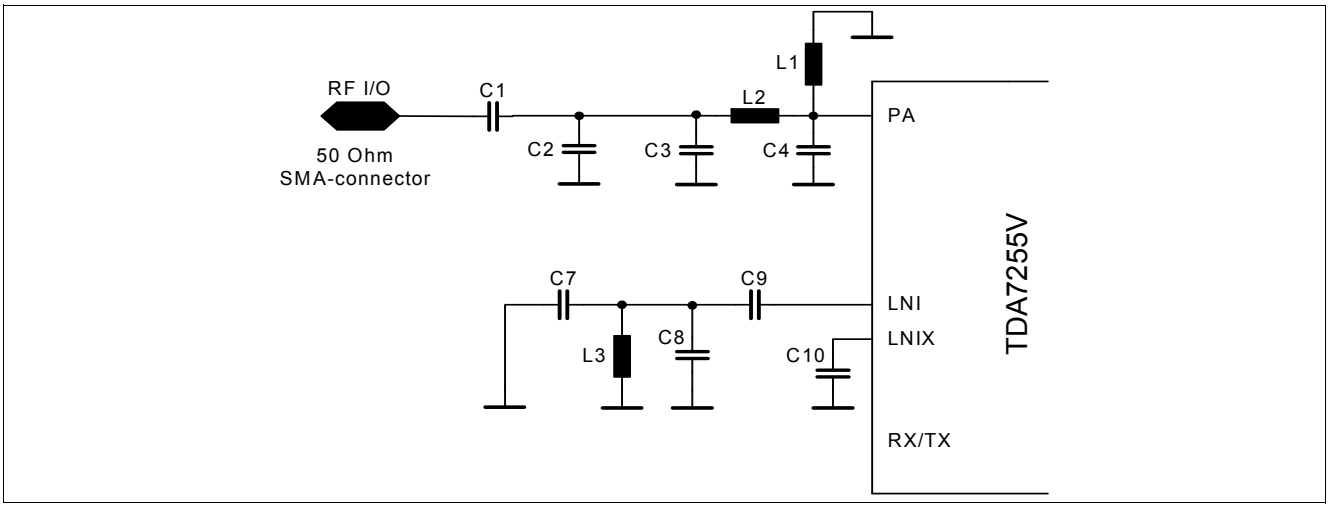


Figure 25 TX_Mode_Simplified

The LNA-matching is RF-grounded now, so no power is lost in the LNA-input. The PA-matching consists of C2, C3, L2, C4 and L1.

When designing the matching of the PA, C2 must not be changed anymore because its value is already fixed by the LNA-input-matching.

3.1.4 Power Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta << \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of **Figure 26**. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.

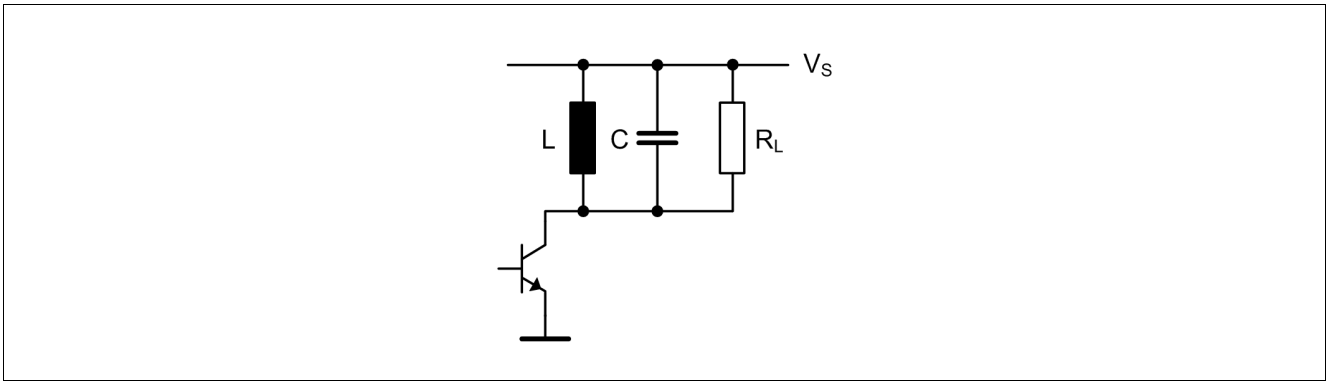


Figure 26 Equivalent Power Amplifier Tank Circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^{\,2}}{2P_0} \tag{9}$$

A typical value of R_{LC} for an RF output power of P_o= 13 mW is:

$$R_{LC} = \frac{3^2}{2 \cdot 0.013} = 350\Omega \tag{10}$$

Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S. The high efficiency under “critical” operating conditions can be explained by the low power loss at the transistor.

During the conducting phase of the transistor there is no or only a very small collector voltage present, thus minimizing the power loss of the transistor (i_C*u_{CE}). This is particularly true for low current flow angles of $\theta << \pi$. In practice the RF-saturation voltage of the PA transistor and other parasitics will reduce the “critical” R_{LC}.

The output power P_o will be reduced when operating in an “overcritical” mode at a $R_L > R_{LC}$. As shown in **Figure 27**, however, power efficiency E (and bandwidth) will increase by some degree when operating at higher R_L. The collector efficiency E is defined as

$$E = \frac{P_O}{V_S I_C} \tag{11}$$

The diagram of **Figure 27** has been measured directly at the PA-output at V_S = 3 V. A power loss in the matching circuit of about 3 dB will decrease the output power. As shown in the diagram, 250 Ω is the optimum impedance for operation at 3 V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those 2 formulas can be used:

$$R_{OPT} \sim V_S \tag{12}$$

and

$$P_{OPT} \sim R_{OPT} \tag{13}$$

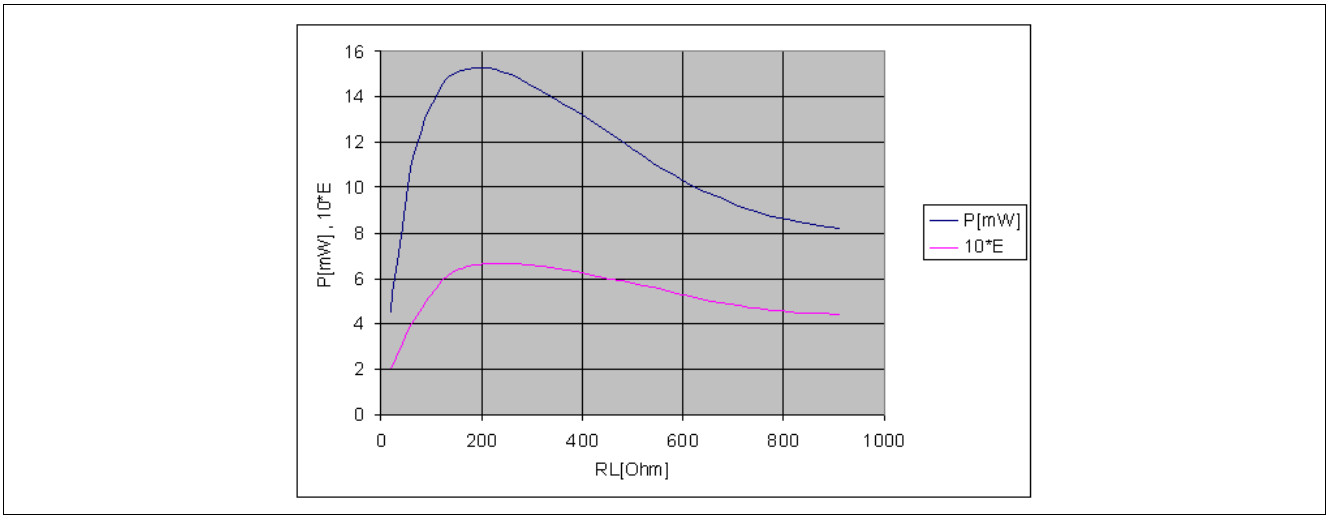


Figure 27 Output Power P_o (mW) and Collector Efficiency E vs. Load Resistor RL

The DC collector current I_c of the power amplifier and the RF output power P_o vary with the load resistor P_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

As **Figure 28** shows, detuning beyond the bandwidth of the matching circuit results in a significant increase of collector current of the power amplifier and in some loss of output power. This diagram shows the data for the circuit of the test board at the frequency of 434 MHz. The effective load resistor of this circuit is R_L = 250 Ω, which is the optimum impedance for operation at 3 V. This will lead to a dip of the collector current f approx. 20%.

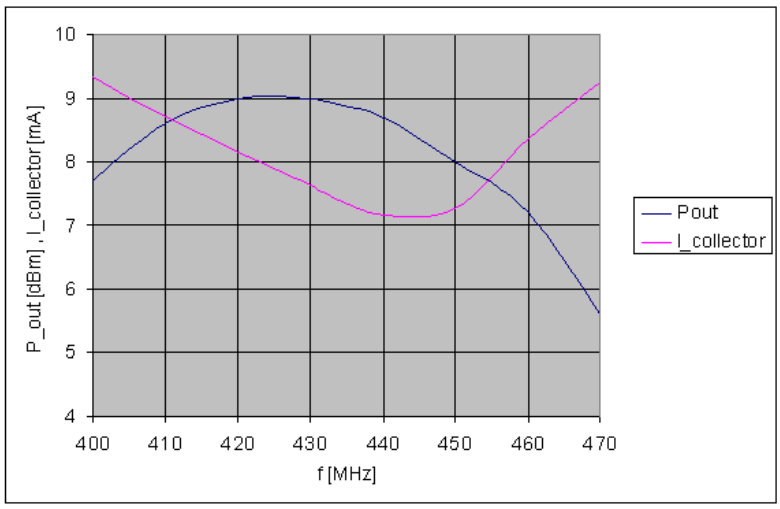


Figure 28 Power Output and Collector Current vs. Frequency

C4, L2 and C3||C2 are the main matching components which are used to transform the 50 Ω load at the SMA-RF-connector to a higher impedance at the PA-output (250 Ω @ 3 V). L1 can be used for fine-tuning of the resonance frequency but should not be too low in order to keep its loss low.

The transformed impedance of 250 Ω+j0 at the PA-output-pin can be verified with a network analyzer using this measurement procedure:

1. Calibrate your network analyzer.
2. Connect a short, low-loss 50 Ω cable to your network analyzer with an open end on one side. Semirigid cable works best.
3. Use the „Port Extension“ feature of your network analyzer to shift the reference plane of your network analyzer to the open end of the cable.
4. Connect the center-conductor of the cable to the solder pad of the pin „PA“ of the IC. The shield has to be grounded. Very short connections must be used. Do not remove the IC or any part of the matching-components!
5. Screw a 50 Ω-dummy-load on the RF-I/O-SMA-connector
6. The TDA7255V has to be in ASK-TX-Mode, Data-Input = LOW.
7. Be sure that your network analyzer is AC-coupled and turn on the power supply of the IC.
8. Measure the S-parameter

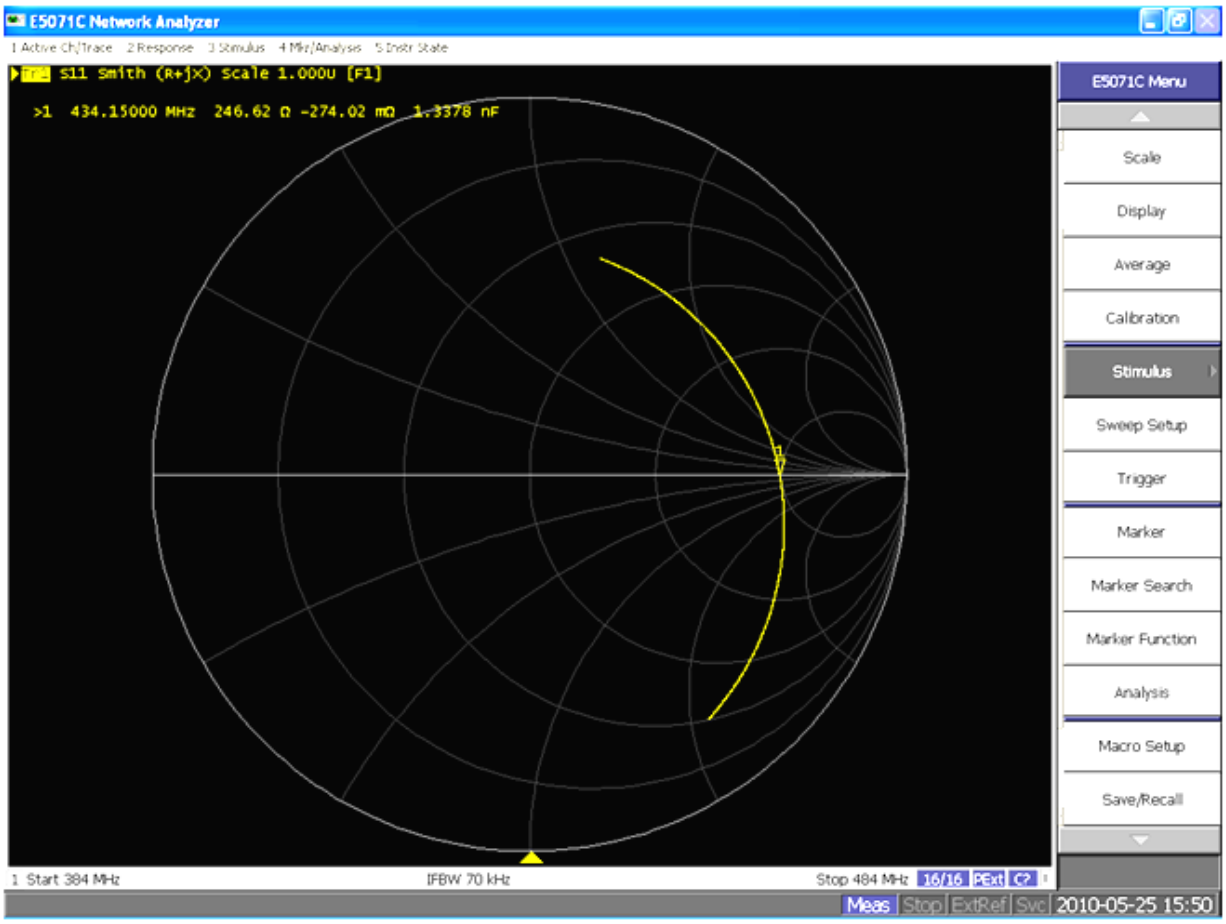


Figure 29 S11-Parameter measured 100 MHz

Above you can see the measurement of the evalboard with a span of 100 MHz. The evalboard has been optimized for 3 V. The load should be about 250+j0 at 434,2 MHz.

A tuning-free realization requires a careful design of the components within the matching network. A simple linear CAE-tool will help to see the influence of tolerances of matching components.

Suppression of spurious harmonics may require some additional filtering within the antenna matching circuit. Both can be seen in **Figure 30** and **Figure 31** The total spectrum of the evalboard can be summarized as:

Carrier f_c	9 dBm
f_c-18.1 MHz	-73 dBm
f_c+18.1 MHz	-76 Bm
2nd harmonic	-43 dBm
3rd harmonic	-43 dBm

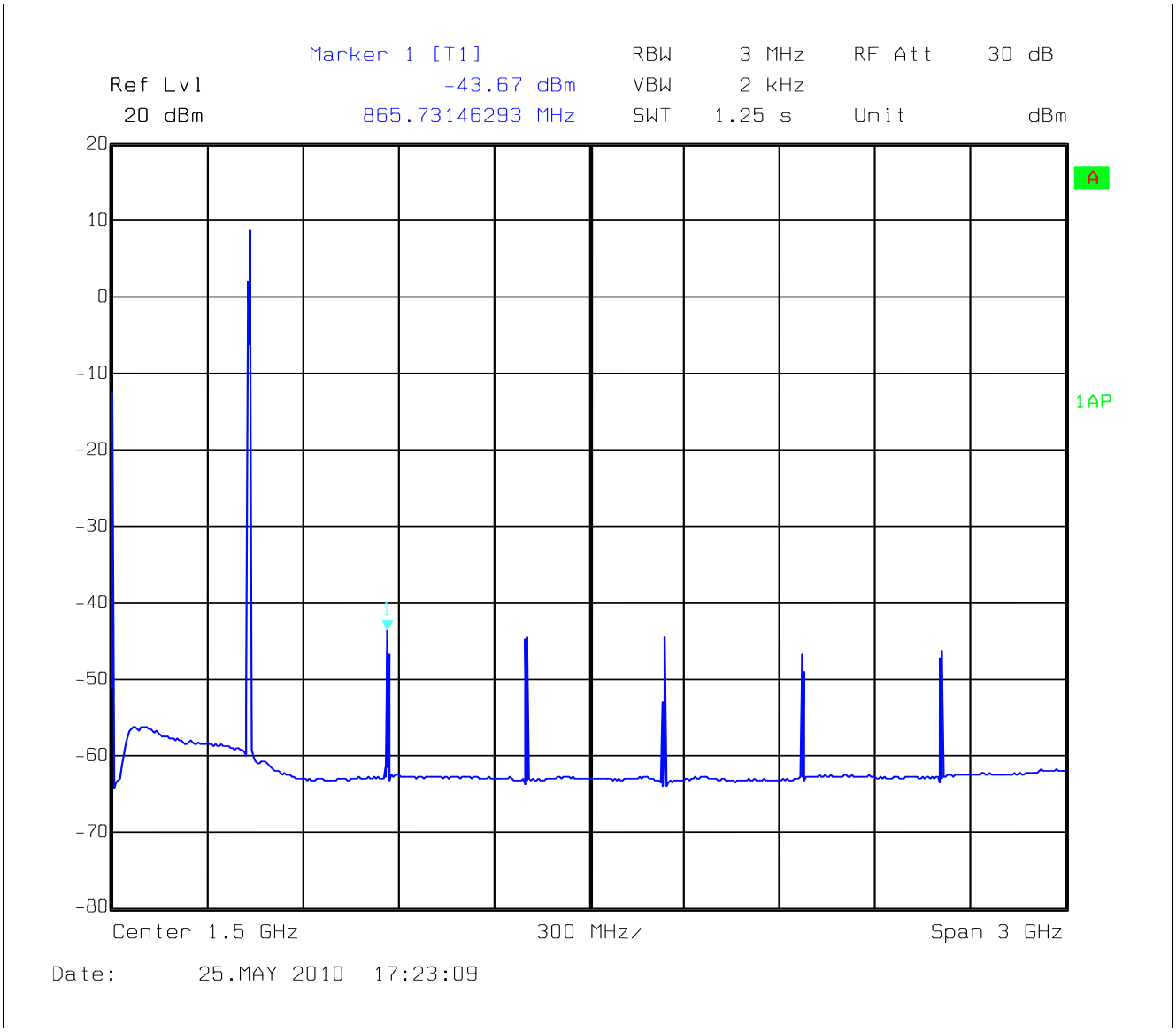


Figure 30 Transmit Spectrum 3 GHz

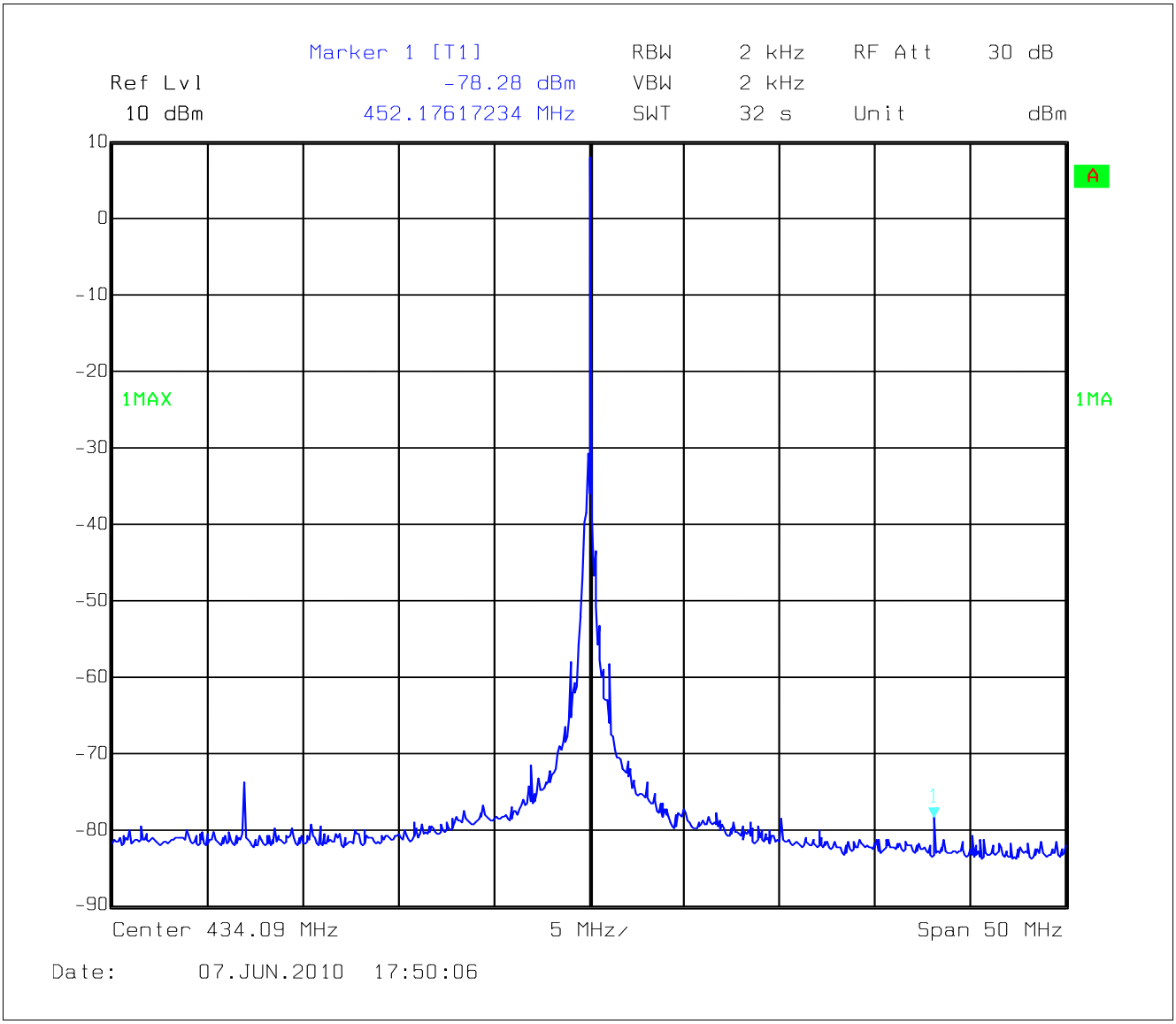


Figure 31 Transmit Spectrum X-tal-Oscillator Spurs

3.2 Crystal Oscillator

The equivalent schematic of the crystal with its parameters specified by the crystal manufacturer can be taken from the subsequent figure.

Here also the load capacitance of the crystal C_L, which the crystal wants to see in order to oscillate at the desired frequency, can be seen.

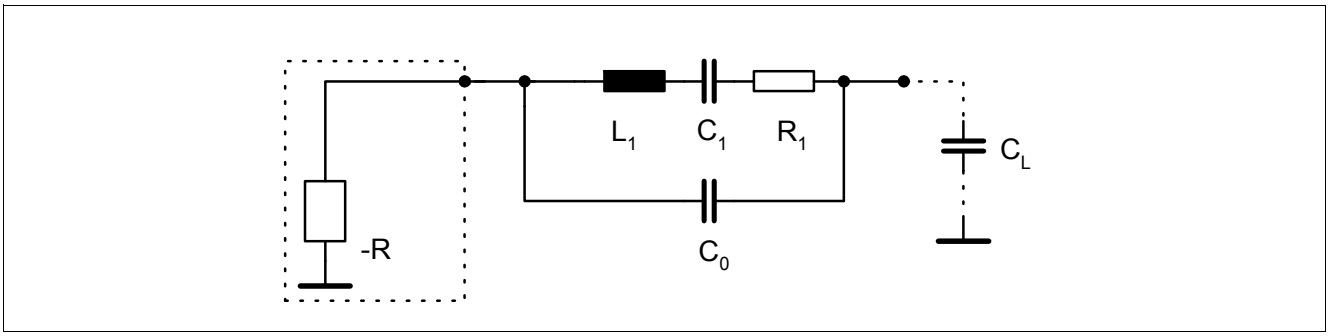


Figure 32 Crystal

L_1 Motional inductance of the crystal

C_1 Motional capacitance of the crystal

C_0 Shunt capacitance of the crystal

Therefore the **Resonant Frequency f_s** of the crystal is defined as:

$$f_S = \frac{1}{2\pi\sqrt{L_1 \cdot C_1}} \tag{14}$$

The **Series Load Resonant Frequency f_s'** of the crystal is defined as:

$$f_S` = \frac{1}{2\pi\sqrt{L_1 \cdot C_1}} \cdot \sqrt{1 + \frac{C_1}{C_0 + C_L}} \tag{15}$$

Regarding **Figure 32**

f_s' is the nominal frequency of the crystal with a specified load when tested by the crystal manufacturer.

Pulling Sensitivity of the crystal is defined as the magnitude of the relative change in frequency relating to the variation of the load capacitor.

$$\frac{\delta D}{\delta C_L} = \frac{\delta f_S' / f_S}{\delta C_L} = \frac{-C_1}{2(C_0 + C_L)^2} \tag{16}$$

Choosing C_L as large as possible results in a small pulling sensitivity. On the other hand a small C_L keeps the influence of the serial inductance and the tolerances associated to it small (see **Equation (18)**).

Start-up Time

$$t_{Start} \sim \frac{L_1}{|-R| - R_{ext}} \quad (17)$$

where: -R Is the negative impedance of the oscillator, see **Figure 33**

R_{ext} Is the sum of all external resistances (e.g. R_1 or any other resistance that may be present in the circuit), see **Figure 32**

The proportionality of L_1 and C_1 of the crystal is defined by **Equation (14)**. For a crystal with a small C_1 the start - up time will also be slower. Typically the lower the value of the crystal frequency, the lower the C_1.

A short **conclusion** regarding crystal and crystal oscillator dependencies is shown in the following table:

Table 21 Crystal and crystal oscillator dependency

	Result		
Independent variable	**Relative Tolerance**	**Maximum Deviation**	**t Start-up**
C_1 >	>>	>>	<
C_0 >	<	<	-
Frequency of quartz >	>>>	>	<<
L_{OSC} >	>>	>	-
C_L >	>	<	-

The crystal oscillator in the TDA7255V is a NIC (negative impedance converter) oscillator type. The input impedance of this oscillator is a negative impedance in series to an inductance. Therefore the load capacitance of the crystal C_L (specified by the crystal supplier) is transformed to the capacitance C_V as shown in **Equation (18)**.

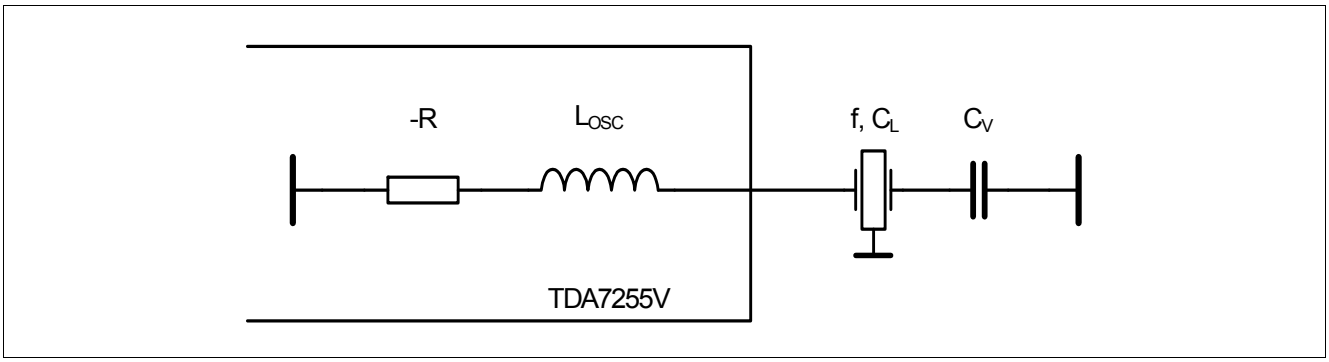


Figure 33 Crystal Oscillator

$$C_L = \frac{1}{\frac{1}{C_V} - \omega^2 L_{OSC}} \leftrightarrow C_V = \frac{1}{\frac{1}{C_L} + \omega^2 L_{OSC}} \quad (18)$$

C_L Crystal load capacitance for nominal frequency

ω Angular frequency

L_{OSC} Inductivity of the crystal oscillator - typ: 2.7 mH with pad of board, 2.45 µH without pad

With the aid of this formula it becomes obvious that the higher the serial capacitance C_v is, the higher is the influence of L_{OSC}.

The tolerance of the internal oscillator inductivity is much higher, so the inductivity is the dominating value for the tolerance.

FSK modulation and tuning are achieved by a variation of C_v.

In case of small frequency deviations (up to +/- 1000 ppm), the desired load capacitances for FSK modulation are frequency depending and can be calculated with the formula below.

$$C_L \pm = \frac{C_L \mp C_0 \cdot \frac{\Delta f}{N \cdot f} \cdot \left(1 + \frac{2 \cdot (C_0 + C_L)}{C_1}\right)}{1 \pm \frac{\Delta f}{N \cdot f}\left(1 + \frac{2 \cdot (C_0 + C_L)}{C_1}\right)} \quad (19)$$

C_L	Crystal load capacitance for nominal frequency
C_0	Shunt capacitance of the crystal
C_1	Motional capacitance of the crystal
f	Crystal oscillator frequency
N	Division ratio of the PLL
Δf	Peak frequency deviation

With C_{L+} and C_{L-} the necessary C_{v+} for FSK HIGH and C_{v-} for FSK LOW can be calculated.

Alternatively, an external AC coupled (10 nF in series to 1 kΩ) signal can be applied at pin 16 (XOUT). The drive level should be approximately 100 mVpp.

3.2.1 Synthesizer Frequency Setting

Generating ASK and FSK modulation 3 settable frequencies are necessary.

3.2.1.1 Possible Crystal Oscillator Frequencies

The resulting possible crystal oscillator frequencies are shown in the following **Figure 34**

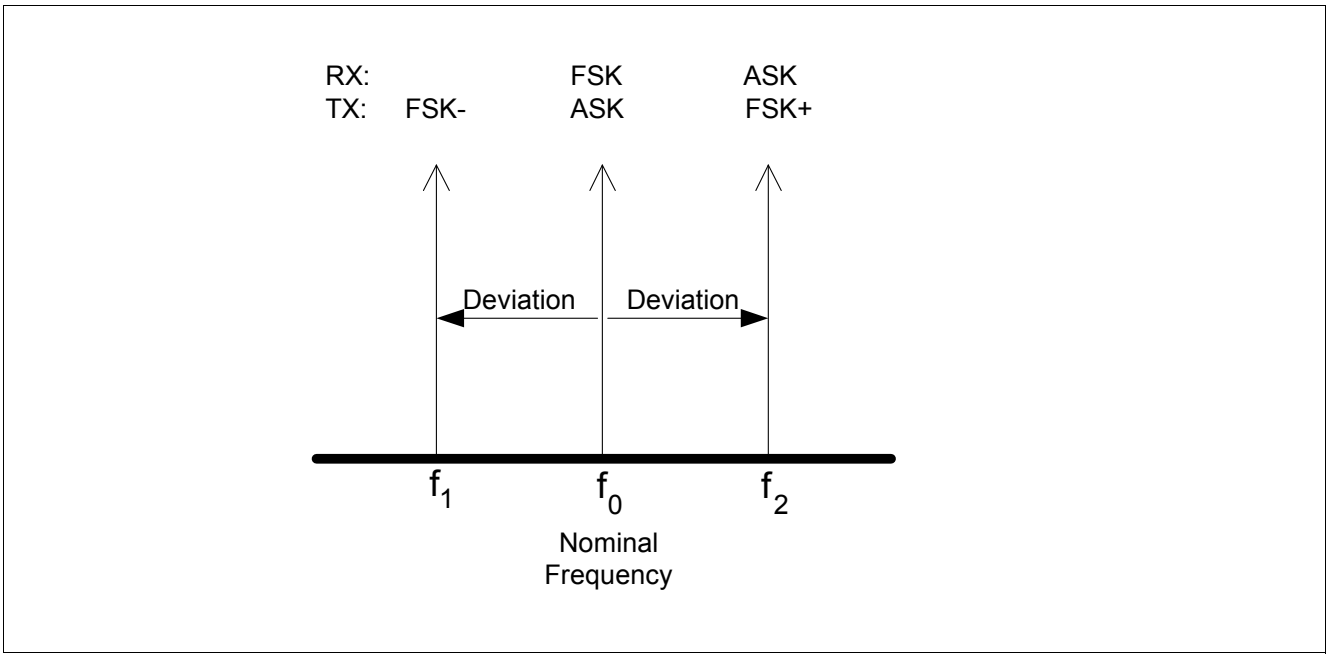


Figure 34 Possible Crystal Oscillator Frequencies

In ASK receive mode the crystal oscillator is set to frequency f_2 to realize the necessary frequency offset to receive the ASK signal at f_0*N (N: division ratio of the PLL).

To set the 3 different frequencies 3 different C_v are necessary. Via internal switches 3 external capacitors can be combined to generate the necessary C_v in case of ASK- or FSK-modulation. Internal banks of switchable capacitors allow the fine-tuning of these frequencies.

3.2.2 Transmit/Receive ASK/FSK Frequency Assignment

Depending on whether the device operates in transmit or receive mode or whether it operates in ASK or FSK the following cases can be distinguished:

3.2.2.1 FSK-Mode

In **transmit** mode the two frequencies representing logical HIGH and LOW data states have to be adjusted depending on the intended frequency deviation and separately according to the following formulas:

$$f_{COSC\ HI} = (f_{RF} + f_{DEV}) / 24 \quad (20)$$

$$f_{COSC\ LOW} = (f_{RF} - f_{DEV}) / 24 \quad (21)$$

e.g.

$f_{COSC\ HI}$ = (434,16E6 + 35E3) / 24 = 18.09146 MHz

$f_{COSC\ LOW}$ = (434,16E6 - 35E3) / 24 = 18.08854 MHz

with a frequency deviation of 35 kHz.

Figure 35 shows the configuration of the switches and the capacitors to achieve the 2 desired frequencies. Gray parts of the schematics indicate inactive parts. For FSK modulation the ASK-switch is always open.

For FSK LOW the FSK-switch is closed and C_{v2} and C_{tune2} are bypassed. The effective C_{v-} is given by:

$$C_{V-} = C_{v1} + C_{tune1} \tag{22}$$

For fine-tuning C_{tune1} can be varied over a range of 8 pF in steps of 125 fF. The switches of this C-bank are controlled by the bits D0 to D5 in the FSK register (sub-address 01H, see **Table 25**).

For FSK HIGH the FSK-switch is open. So the effective C_{v+} is given by:

$$C_{V+} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{V2} + C_{tune2})}{C_{V1} + C_{tune1} + C_{V2} + C_{tune2}} \tag{23}$$

The C-bank C_{tune2} can be varied over a range of 16 pF in steps of 250 fF for fine-tuning of the FSK HIGH frequency. The switches of this C-bank are controlled by the bits **D8** to **D13** in the **FSK** register (sub-address 01H, see **Table 25**).

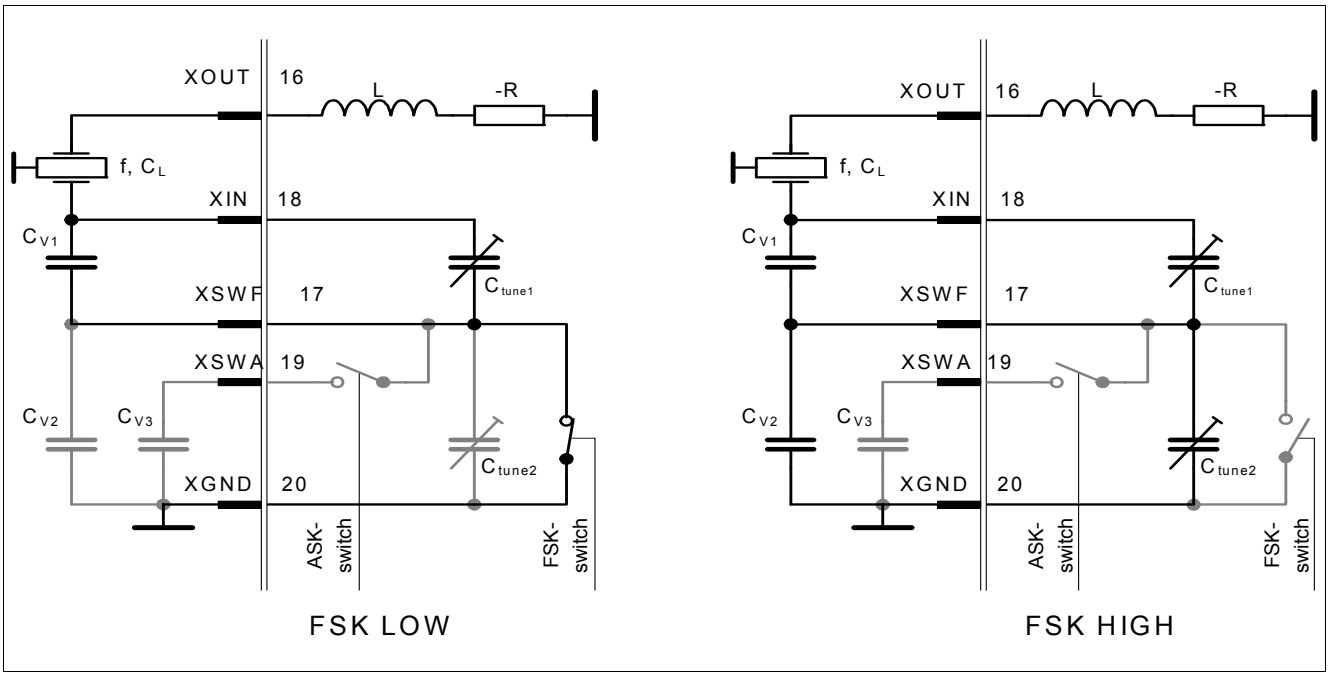


Figure 35 FSK Modulation

In receive mode the crystal oscillator frequency is set to yield a direct-to-zero conversion of the receive data. Thus the frequency may be calculated as

$f_{COSC} = f_{RF} / 24$, (24)

e.g.

f_{COSC} = 434,15E6 / 24= 18.089583 MHz

which is identical to the ASK transmit case.

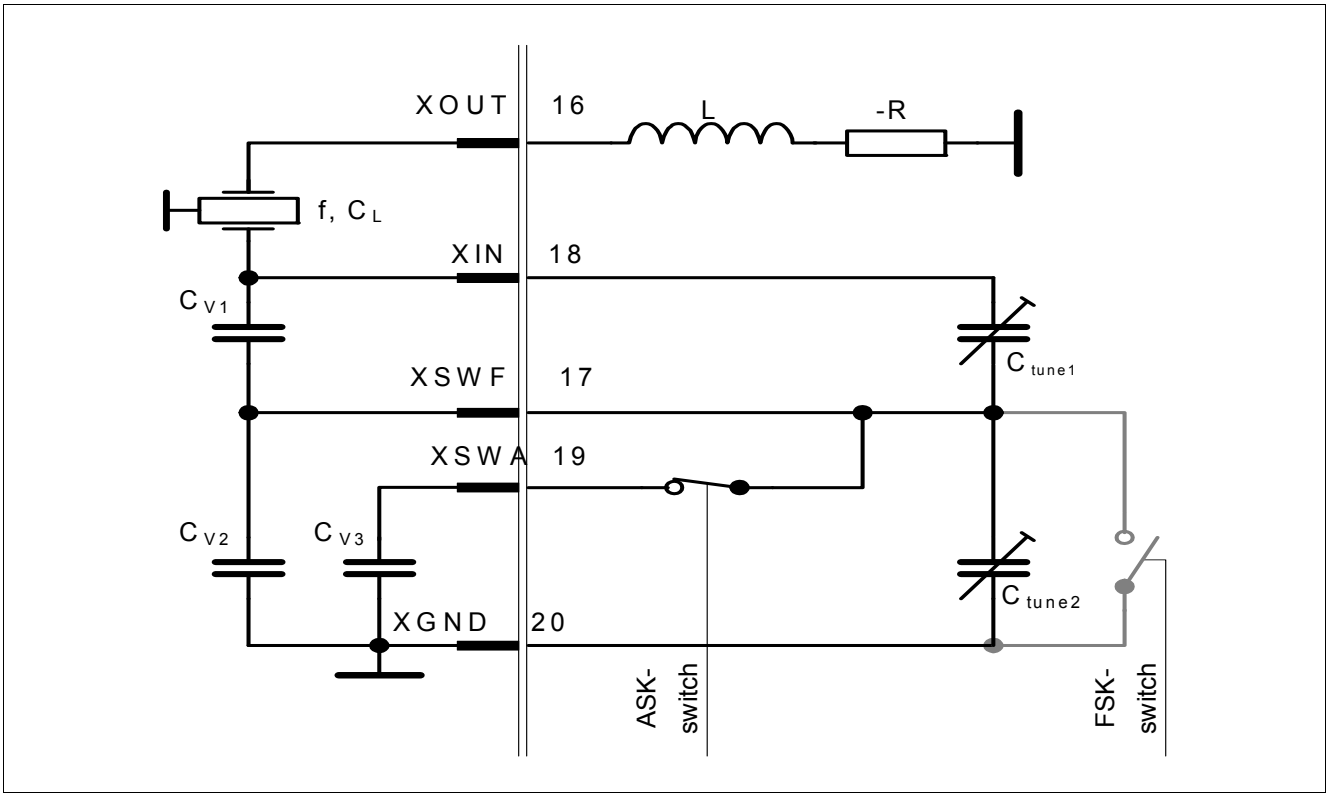


Figure 36 FSK Receive

In this case the ASK-switch is closed. The necessary C_{vm} is given by:

$$C_{V+} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{V2} + C_{V3} + C_{tune2})}{C_{V1} + C_{tune1} + C_{V2} + C_{V3} + C_{tune2}} \quad (25)$$

The C-bank C_{tune2} can be varied over a range of 16 pF in steps of 250 fF for fine-tuning of the FSK receive frequency. In this case the switches of the C-bank are controlled by the bits D0 to D5 of the XTAL_TUNING register (sub-address 02H, see **Table 24**).

3.2.2.2 ASK-Mode

In transmit mode the crystal oscillator frequency is the same as in the FSK receive case, **Figure 36**.

In receive mode a receive frequency offset is necessary as the limiters feedback is AC-coupled. This offset is achieved by setting the oscillator frequency to the FSK HIGH transmit frequency, **Figure 35**.

3.2.3 Parasitics

For the correct calculation of the external capacitors the parasitic capacitances of the pins and the switches (C_{20}, C_{21}, C_{22}) have to be taken into account.

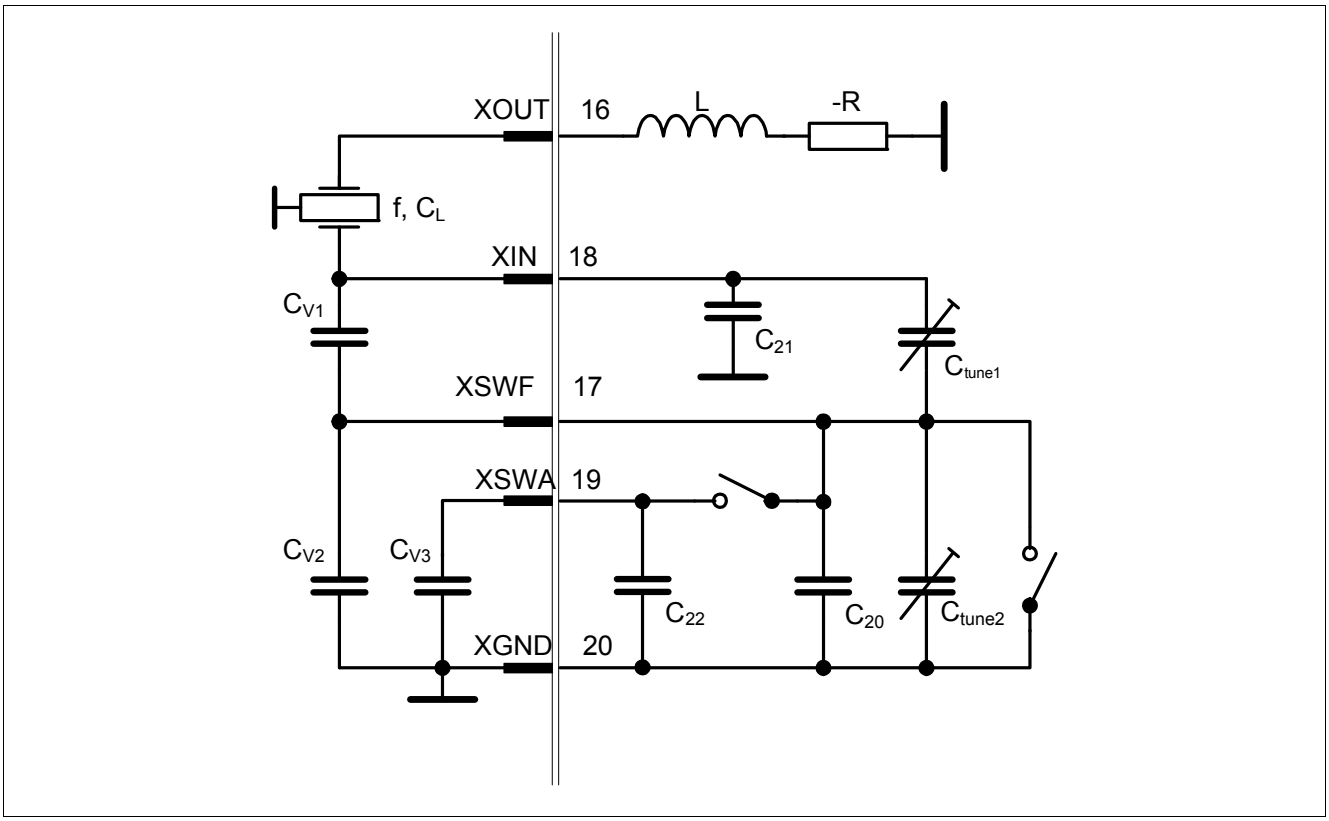


Figure 37 Parasitics of the Switching Network

Table 22 Typical Values of Parasitic Capacitances

Name	Value
C_{20}	4,6 pF
C_{21}	FSK_Low: 2,8 pF / FSK_High & ASK: 2.2 pF
C_{22}	1 pF

With the given parasitics the actual C_v can be calculated:

$$C_{V-} = C_{V1} + C_{tune1} + C_{21} \tag{26}$$

$$C_{V+} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{V2} + C_{20} + C_{tune2})}{C_{V1} + C_{tune1} + C_{V2} + C_{20} + C_{tune2}} + C_{21} \tag{27}$$

$$C_{vm} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{V2} + C_{20} + C_{V3} + C_{22} + C_{tune2})}{C_{V1} + C_{tune1} + C_{V2} + C_{20} + C_{V3} + C_{22} + C_{tune2}} + C_{21} \tag{28}$$

Note: Please keep in mind also to include the Pad parasitics of the circuit board.

3.2.4 Calculation of the External Capacitors

- Determination of necessary crystal frequency using **Equation (20)**
  e.g. $f_{FSK-} = f_{COSC\ LOW}$
- Determine corresponding C_{Load} applying **Equation (19)**
  e.g. $C_{L\ FSK-} = C_{L\pm}$
- Necessary C_v using **Equation (18)**
  e.g.

$$C_{V-} = \frac{1}{\frac{1}{C_{L,FSK-}} + (2\pi f_{FSK-})^2 \cdot L_{OSC}} \tag{29}$$

- When the necessary C_v for the 3 frequencies (C_v for FSK LOW, C_{v+} for FSK HIGH and C_{vm} for FSK-receive) are known the external capacitors and the internal tuning caps can be calculated using the following formulas:

-FSK:

$$C_{v1} + C_{tune1} = C_{v-} - C_{21} \tag{30}$$

-FSK:

$$C_{V2} + C_{tune2} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{V+} - C_{21})}{(C_{V1} + C_{tune1}) - (C_{V+} - C_{21})} - C_{20} \tag{31}$$

FSK_RX:

$$C_{V3} + C_{tune2} = \frac{(C_{V1} + C_{tune1}) \cdot (C_{Vm} - C_{21})}{(C_{V1} + C_{tune1}) - (C_{Vm} - C_{21})} - C_{20} - C_{V2} - C_{22} \tag{32}$$

To compensate frequency errors due to crystal and component tolerance C_{v1}, C_{v2} and C_{v3} have to be varied. To enable this correction, half of the necessary capacitance variation has to be realized with the internal C-banks.

If no fine-tuning is intended it is recommended to leave XIN (Pin 18) open. So the parasitic capacitance of Pin 18 has no effect.

Please keep in mind also to include the Pad parasitics of the circuit board.

In the suitable range for the serial capacitor, either capacitors with a tolerance of 0.1 pF or 1% are available.

A spreadsheet, which can be used to predict the total frequency error by simply entering the crystal specification, may be obtained from Infineon.

3.2.5 FSK-Switch Modes

The FSK-switch can be used either in a bipolar or in a FET mode. The mode of this switch is controlled by bit D0 of the XTAL_CONFIG register (sub-address 0EH).

In the bipolar mode the FSK-switch can be controlled by a ramp function. This ramp function is set by the bits D1 and D2 of the XTAL_CONFIG register (sub-address 0EH). With these modes of the FSK-switch the bandwidth of the FSK spectrum can be influenced.

When working in the FET mode the power consumption can be reduced by about 200 µA.

The default mode is bipolar switch with no ramp function (D0 = 1, D1 = D2 = 0), which is suitable for all bitrates.

Table 23 Sub Address $0E_H$: XTAL_CONFIG

D0	D1	D2	Switch mode	Ramp time	Max. Bitrate
0	N.a.	N.a.	FET	< 0.2 µs	> 32 kBit/s NRZ
1	0	0	Bipolar (default)	< 0.2 µs	> 32 kBit/s NRZ
1	1	0	Bipolar	4 µs	32 kBit/s NRZ
1	0	1	Bipolar	8 µs	16 kBit/s NRZ
1	1	1	Bipolar	12 µs	12 kBit/s NRZ

3.2.6 Fine-tuning and FSK Modulation Relevant Registers

Case **FSK-RX** or **ASK-TX** (C_{tune2}):

Table 24 Sub Address 02_H: XTAL_TUNING

Bit	Function	Value	Description	Default
D5	Nominal_Frequ_5	8 pF	Setting for nominal frequency ASK-TX FSK-RX (C_{tune2})	0
D4	Nominal_Frequ_4	4 pF		1
D3	Nominal_Frequ_3	2 pF		0
D2	Nominal_Frequ_2	1 pF		0
D1	Nominal_Frequ_1	500 fF		1
D0	Nominal_Frequ_0	250 fF		0

Case FSK-TX or ASK-RX (C_{tune1} and C_{tune2})

Table 25 Sub Address 01_H: FSK

Bit	Function	Value	Description	Default
D13	FSK_High_5	8 pF	Setting for positive frequency shift: ASK-RX or FSK_High (C_{tune2})	0
D12	FSK_High_4	4 pF		0
D11	FSK_High_3	2 pF		1
D10	FSK_High_2	1 pF		0
D9	FSK_High_1	500 fF		1
D8	FSK_High_0	250 fF		0

Table 25 Sub Address 01_H: FSK (cont'd)

Bit	Function	Value	Description	Default
D5	FSK_Low_5	4 pF	Setting for negative frequency shift: FSK_Low (C_{tune2})	0
D4	FSK_Low_4	2 pF		0
D3	FSK_Low_3	1 pF		1
D2	FSK_Low_2	500 fF		1
D1	FSK_Low_1	250 fF		0
D0	FSK_Low_0	125 fF		0

Default Values

In case of using the evaluation board, the crystal with its typical parameters (fp' = fs' = 18.089583 MHz, C_1 = 8 fF, C_0 = 2,1 pF, C_L = 20 pF) and external capacitors with C_{v1} = 12 pF, C_{v2} = 3.3 pF, C_{v3} = 15 pF each are used the following default states are set in the device.

Table 26 Default Oscillator Settings

Operating State	Frequency
ASK-TX / FSK-RX	434.15 MHz
FSK_High-TX / ASK-RX	+35 kHz
FSK_Low-TX	-35 kHz

3.2.7 Chip and System Tolerances

Quartz: fp' = fs' = 18.089583 MHz; C_1 = 8 fF; C_0 = 2,1 pF; C_L = 20 pF (typical values)

C_{v1} = 12 pF, C_{v2} = 3.3 pF, C_{v3} = 15 pF

Table 27 Internal Tuning

Part	Frequency Tlerance @ 434 MHz	Rel. Tolerance
Frequency set accuracy	+/- 1.3 kHz	+/- 3 ppm
Temperature (-40...+85 C)	+/- 3.5 kHz	+/- 8 ppm
Supply Voltage(2.1...5.5 V)	+/- 0.9 kHz	+/- 2 ppm
Total	+/- 5.7 kHz	+/- 13 ppm

Table 28 Default Setup (without Internal Tuning & without Pin21 Usage)

Part	Frequency Tolerance @ 434 MHz	Rel. Tolerance
Internal capacitors (+/- 10%)	+/- 3.5 kHz	+/- 8 ppm
Inductivity of the crystal oscillator	+/- 11.4 kHz	+/- 26 ppm
Temperature (-40...+85°C)	+/- 3.5 kHz	+/- 8 ppm
Supply Voltage (2.1...5.5 V)	+/- 0.9 kHz	+/- 2 ppm
Total	+/- 19.3 kHz	+/- 44 ppm

Tolerance values in **Table 27** are valid, if pin 21 is not connected. Establishing the connection to pin 21 the tolerances increase by +/- 27 ppm (internal capacitors), if internal tuning is not used.

Concerning the frequency tolerances of the whole system also crystal tolerances (tuning tolerances, temperature stability, tolerance of C_L) have to be considered.

In addition to the chip tolerances also the crystal and external component tolerances have to be considered in the tuning and non-tuning case.

In case of internal tuning: The crystal on the evaluation board has a temperature stability of +/- 20 ppm (or +/- 8.7 kHz), which must be added to the total tolerances in worst case. It's possible to choose a crystal compensating the oscillators temperature drift in a certain range and thus the overall temperature tolerances are minimized.

In case of default setup (without internal tuning and without usage of pin 18) the temperature stability and tuning tolerance of the crystal as well as the tolerance of the external capacitors (+/- 0.1 pF) have to be added. The crystal on the evaluation board has a temperature stability of +/- 20 ppm (or +/- 8.7 kHz) and a tuning tolerance of +/- 10 ppm (or +/- 4.4 kHz). The external capacitors add a tolerance of +/- 3.5 ppm (or +/- 1.5 kHz). Here also the overall temperature tolerances can be reduced when applying an appropriate temperature drift of the crystal.

The frequency stabilities of both the receiver and the transmitter and the modulation bandwidth set the limit for the bandwidth of the IQ filter. To achieve a high receiver sensitivity and efficient suppression of adjacent interference signals, the narrowest possible IQ bandwidth should be realized (see **Chapter 3.3**).

3.3 IQ-Filter

The IQ-Filter should be set to values corresponding to the RF-bandwidth of the received RF signal via the D1 to D3 bits of the LPF register (sub-address 03H).

Table 29 3dB Cutoff Frequencies I/Q Filter

D3	D2	D1	Nominal f_{-3dB} in kHz (programmable)	Resulting effective channel bandwidth in kHz
0	0	0	Not used	
0	0	1	350	700
0	1	0	250	500
0	1	1	200	400
1	0	0	150 (default)	300
1	0	1	100	200
1	1	0	50	100
1	1	1	Not used	

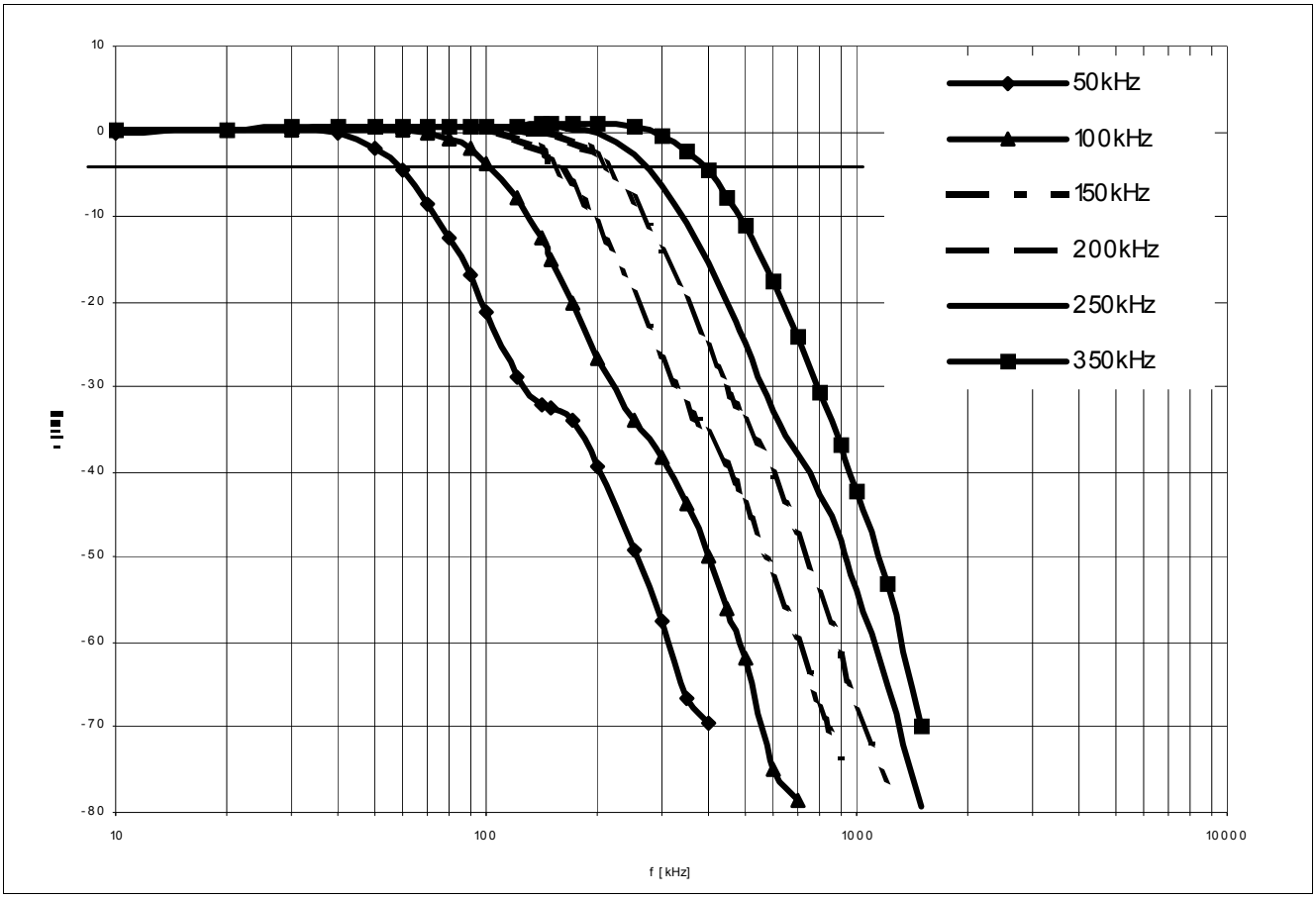


Figure 38 I/Q Filter Characteristics

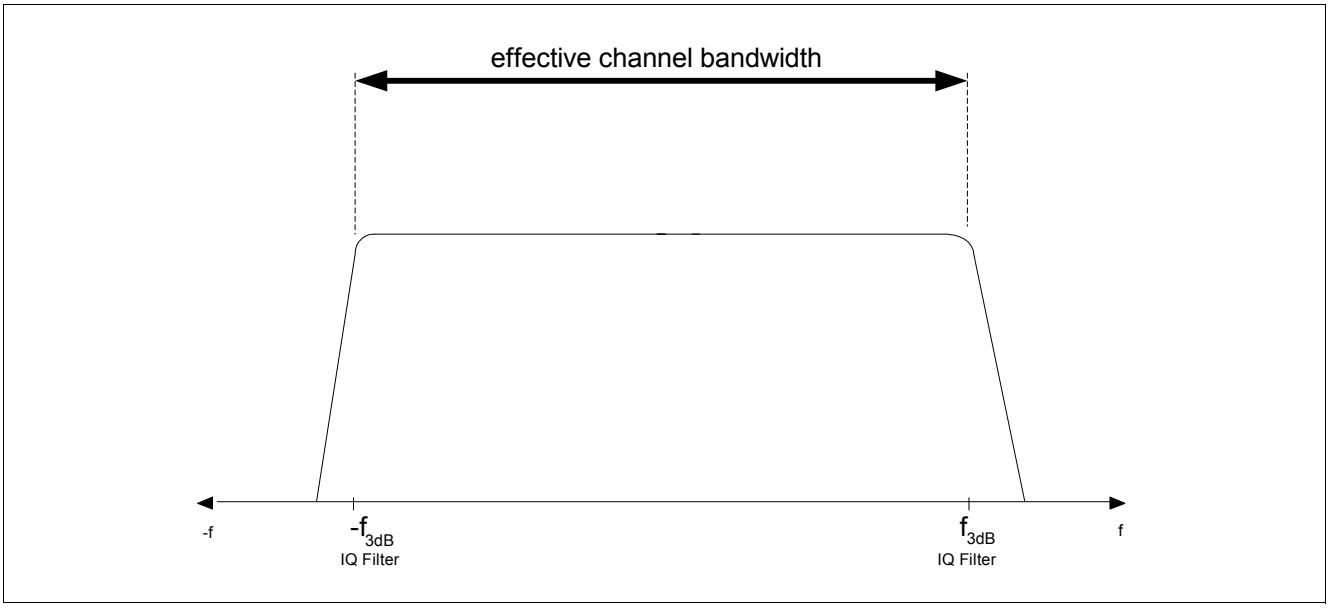


Figure 39 IQ Filter and Frequency Characteristics of the Receive System

3.4 Data Filter

The Data-Filter should be set to values corresponding to the bandwidth of the transmitted Data signal via the D4 to D7 bits of the LPF register (sub-address 03H).

Table 30 3 dB Cutoff Frequencies Data Filter

D7	D6	D5	D4	Nominal f_{-3dB} in kHz
0	0	0	0	5
0	0	0	1	7 (default)
0	0	1	0	9
0	0	1	1	11
0	1	0	0	14
0	1	0	1	18
0	1	1	0	23
0	1	1	1	28
1	0	0	0	32
1	0	0	1	39
1	0	1	0	49
1	0	1	1	55
1	1	0	0	64
1	1	0	1	73
1	1	1	0	86
1	1	1	1	102

3.5 Limiter and RSSI

The I/Q Limiters are DC coupled multistage amplifiers with offset-compensating feedback circuit and an overall gain of approximately 80 dB each in the frequency range of 100 Hz up to 350 kHz. Receive Signal Strength Indicator (RSSI) generators are included in both limiters which produce DC voltages that are directly proportional to the input signal level in the respective channels. The resulting I- and Q-channel RSSI-signals are summed to the nominal RSSI signal.

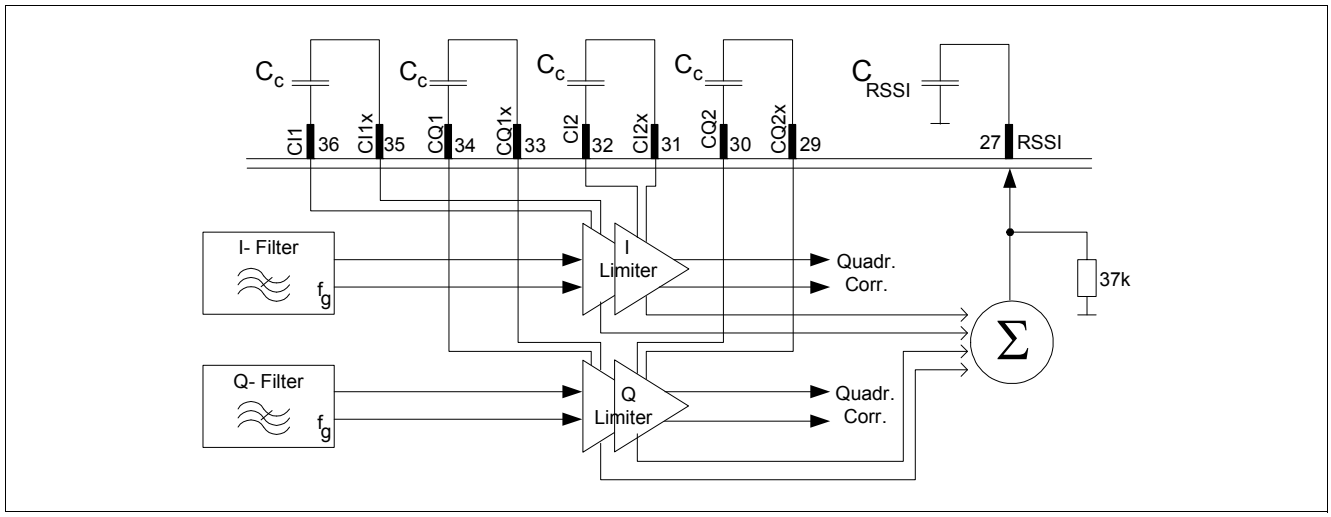


Figure 40 Limiter and Pinning

The DC offset compensation needs 2.2 ms after Power On or Tx/Rx switch. This time is hard wired and independent from external capacitors CC on pins 29 to 36. The maximum value for this capacitors is 47 nF.

RSSI accuracy settling time = 2.2 ms + 5*RC = 2.2 ms + 5*37k*2.2 nF = 2.6 ms

R - Internal resistor

C - External capacitor at Pin 27

Table 31 Limiter Bandwidth

C_c [nF]	f_{3dB} Lower Limit [Hz]	f_{3dB} Upper Limit	Comment
220	100	IQ Filter	Setup time not guaranteed
100	220	- II -	Setup time not guaranteed
47	**470**	**- II -**	**Eval Board**
22	1000	- II -	
10	2200	- II -	

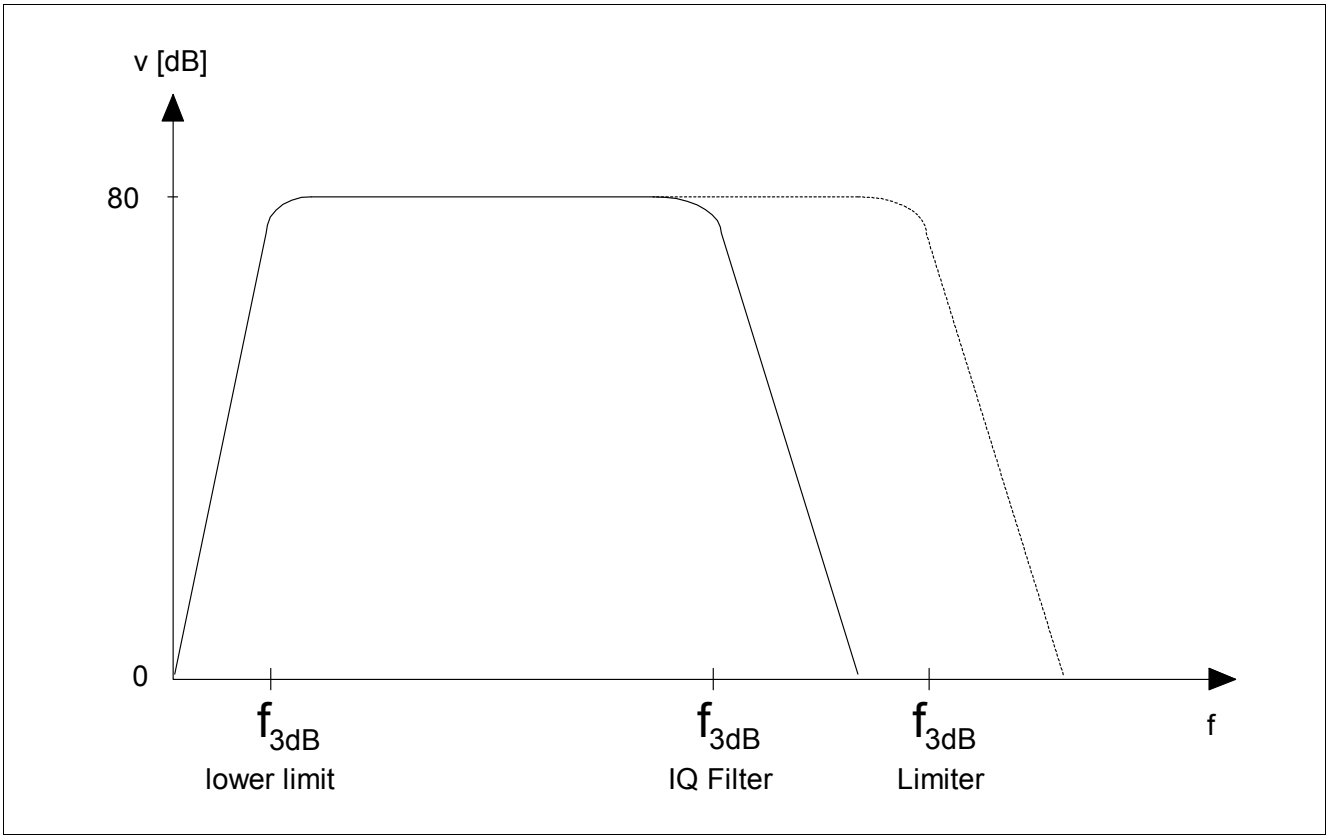


Figure 41 Limiter Frequency Characteristics

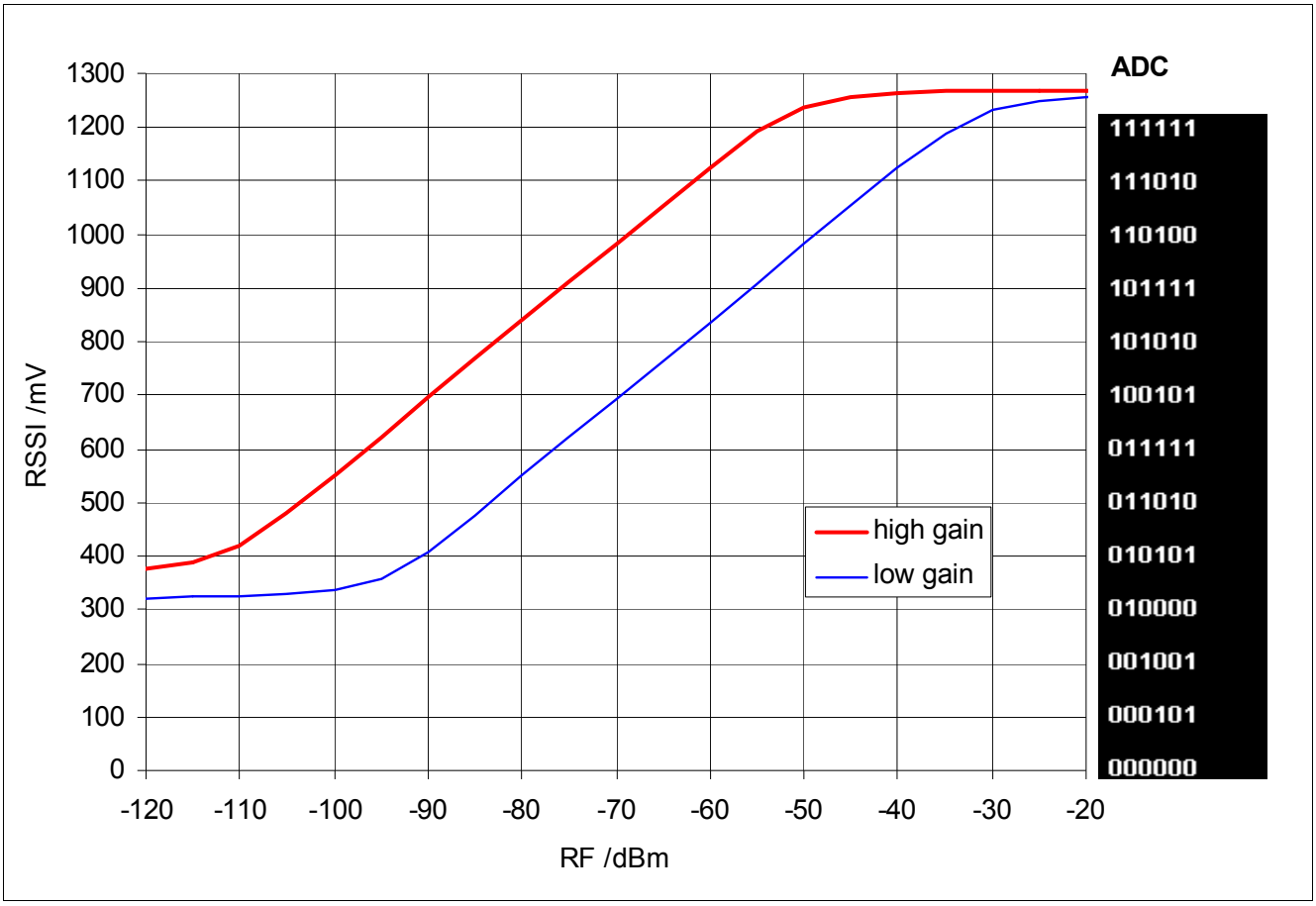


Figure 42 Typ. RSSI Level (Eval Board) @ 3 V

3.6 Data Slicer - Slicing Level

The data slicer is an analog-to-digital converter. It is necessary to generate a threshold value for the negative comparator input (data slicer). The TDA7255V offers an RC integrator and a peak detector which can be selected via logic. Independent of the choice, the peak detector outputs are always active.

3.6.1 RC Integrator

Table 32 Sub Address 00H: CONFIG

Bit	Function	Description	Default	SET
D15	SLICER	0 = LP, 1 = Peak Detector	0	0

Necessary External Component (Pin10): C_{SLC}

This integrator generates the mean value of the data filter output. For a stable threshold value, the cut-off frequency has to be lower than the lowest signal frequency. The cutoff frequency results from the internal resistance R = 100 kΩ and the external capacitor C_{SLC} on Pin10.

Cut-off frequency:

$$f_{cut-off} = \frac{1}{2\pi \cdot 100k\Omega \cdot C_{SLC}} < Min\{f_{Signal}\} \quad (33)$$

Component calculation: (rule of thumb)

T_L – longest period of no signal change

$$C_{SLC} \geq \frac{3 \cdot T_L}{100k\Omega} \quad (34)$$

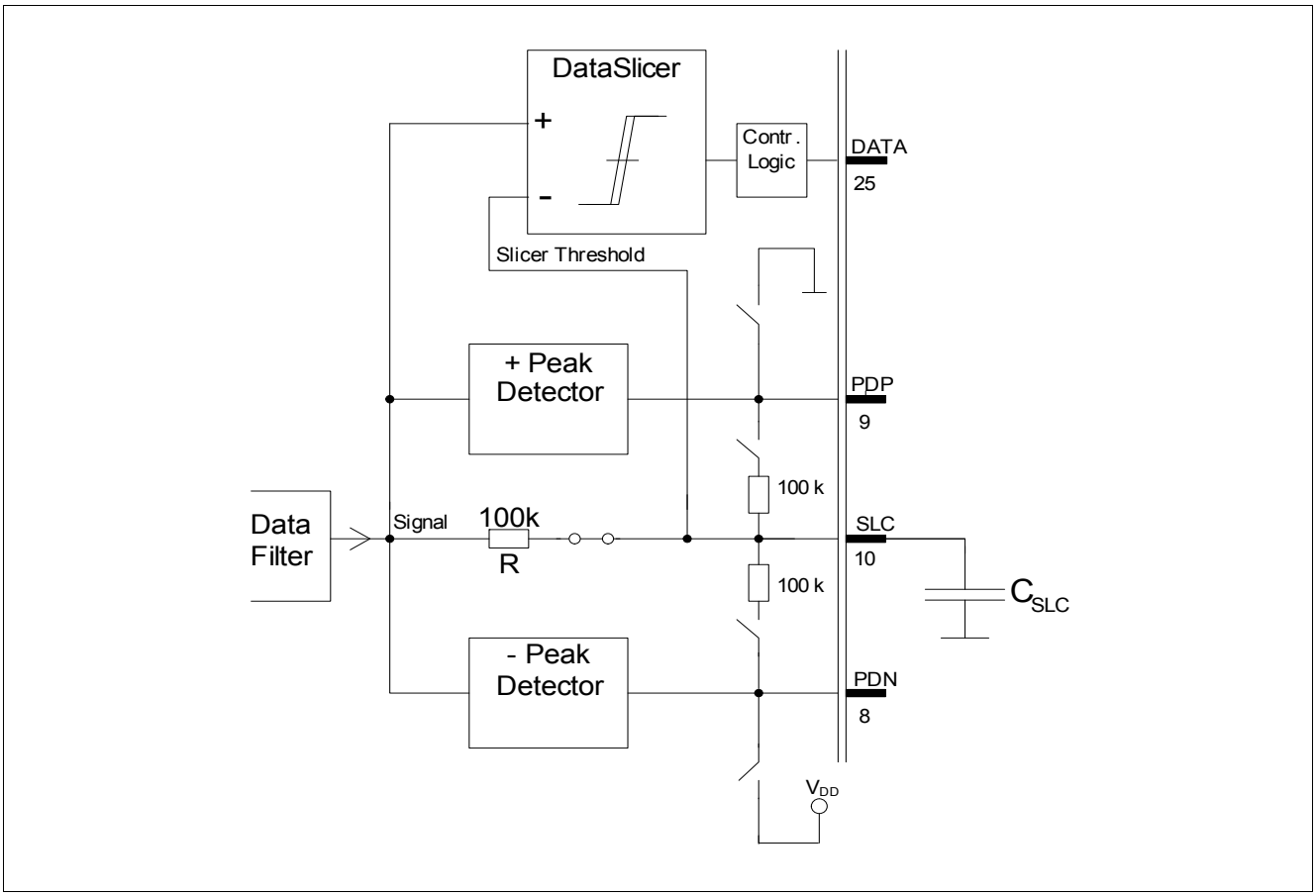


Figure 43 Slicer Level using RC Integrator

3.6.2 Peak Detectors

Table 33 Sub Address 00H: CONFIG

Bit	Function	Description	Default	SET
D15	SLICER	0 = LP, 1 = Peak Detector	0	1

The TDA7255V has two peak detectors built in, one for positive peaks in the data stream and the other for the negative ones.

Necessary External Components

Pin 8: C_N

Pin 9: C_P

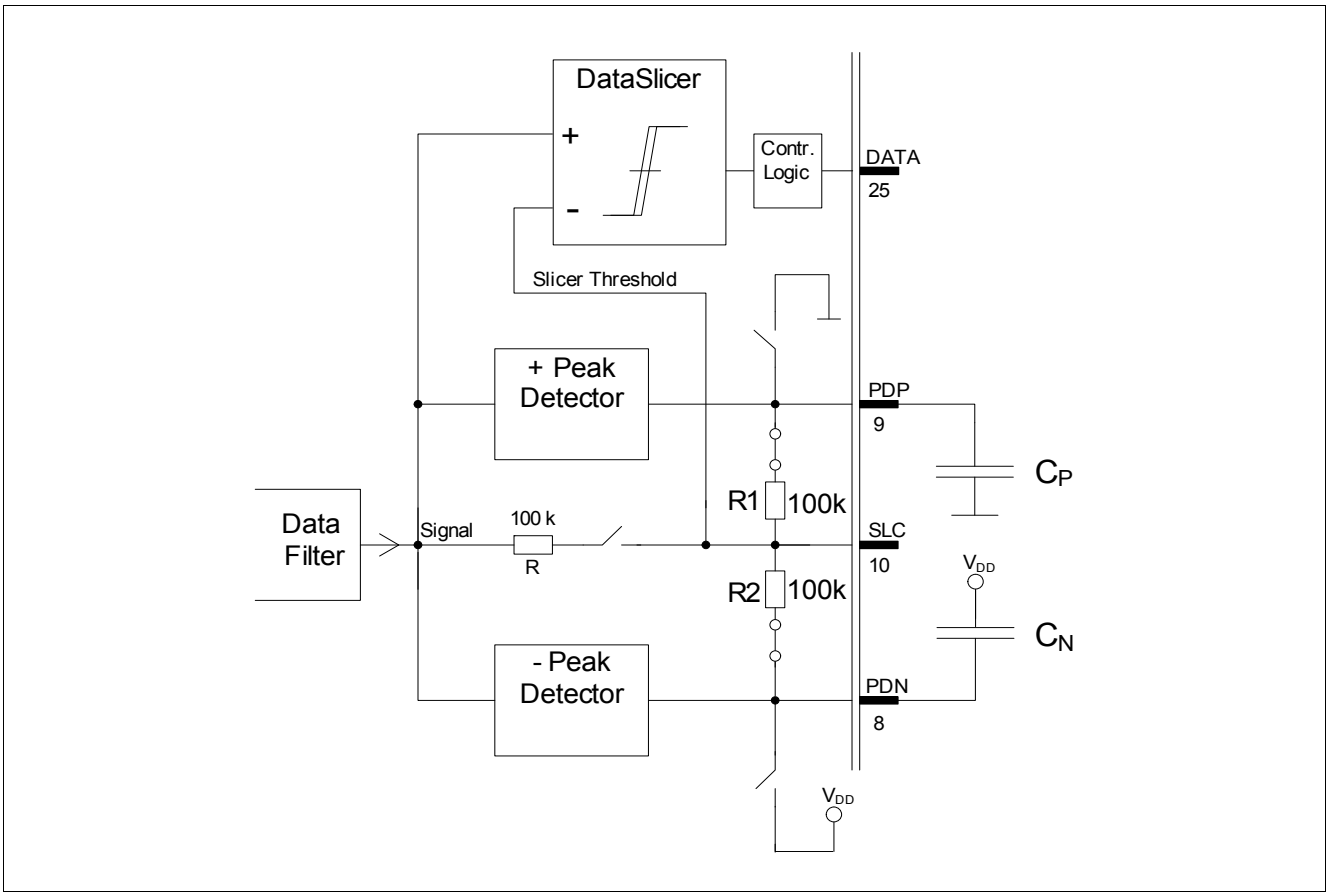


Figure 44 Slicer Level using Peak Detector

For applications requiring fast attack and slow release from the threshold value it is reasonable to use the peak detectors. The threshold value is generated by an internal voltage divider. The release time is defined by the internal resistance values and the external capacitors

$$\tau_{posPkD} = 100k\Omega \cdot C_p \quad (35)$$

$$\tau_{negPkD} = 100k\Omega \cdot C_n \quad (36)$$

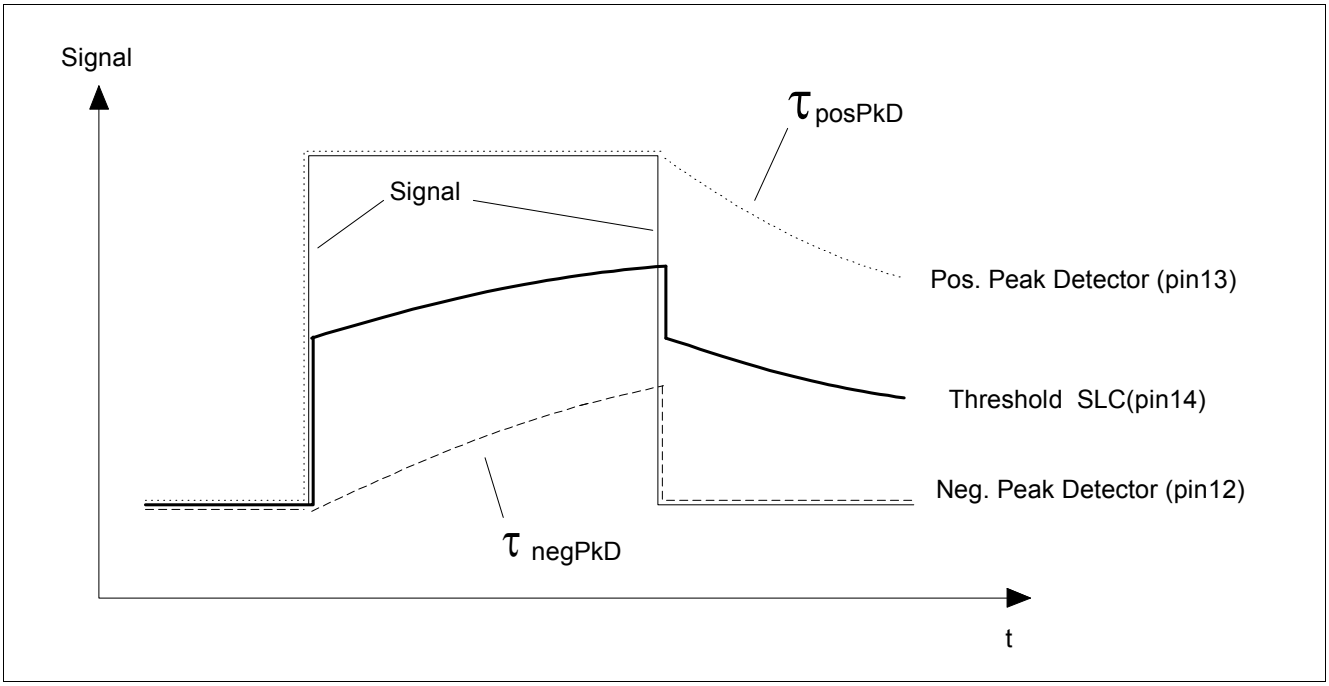


Figure 45 Peak Detector Timing

Component calculation: (rule of thumb)

$$C_p \geq \frac{2 \cdot T_{L1}}{100k\Omega} \tag{37}$$

T_{L1} – longest period of no signal change (LOW signal)

$$C_n \geq \frac{2 \cdot T_{L2}}{100k\Omega} \tag{38}$$

T_{L2} – longest period of no signal change (HIGH signal)

3.6.3 Peak Detector - Analog Output Signal

The TDA7255V data output can be digital (pin 25) or in analog form by using the peak detector output and changing some settings.

To get an analog data output the slicer must be set to **lowpass mode (Reg. 0, D15 = LP = 0)** and the peak detector capacitor at pin 8 or 9 has to be changed to a resistor of about 47 kΩ.

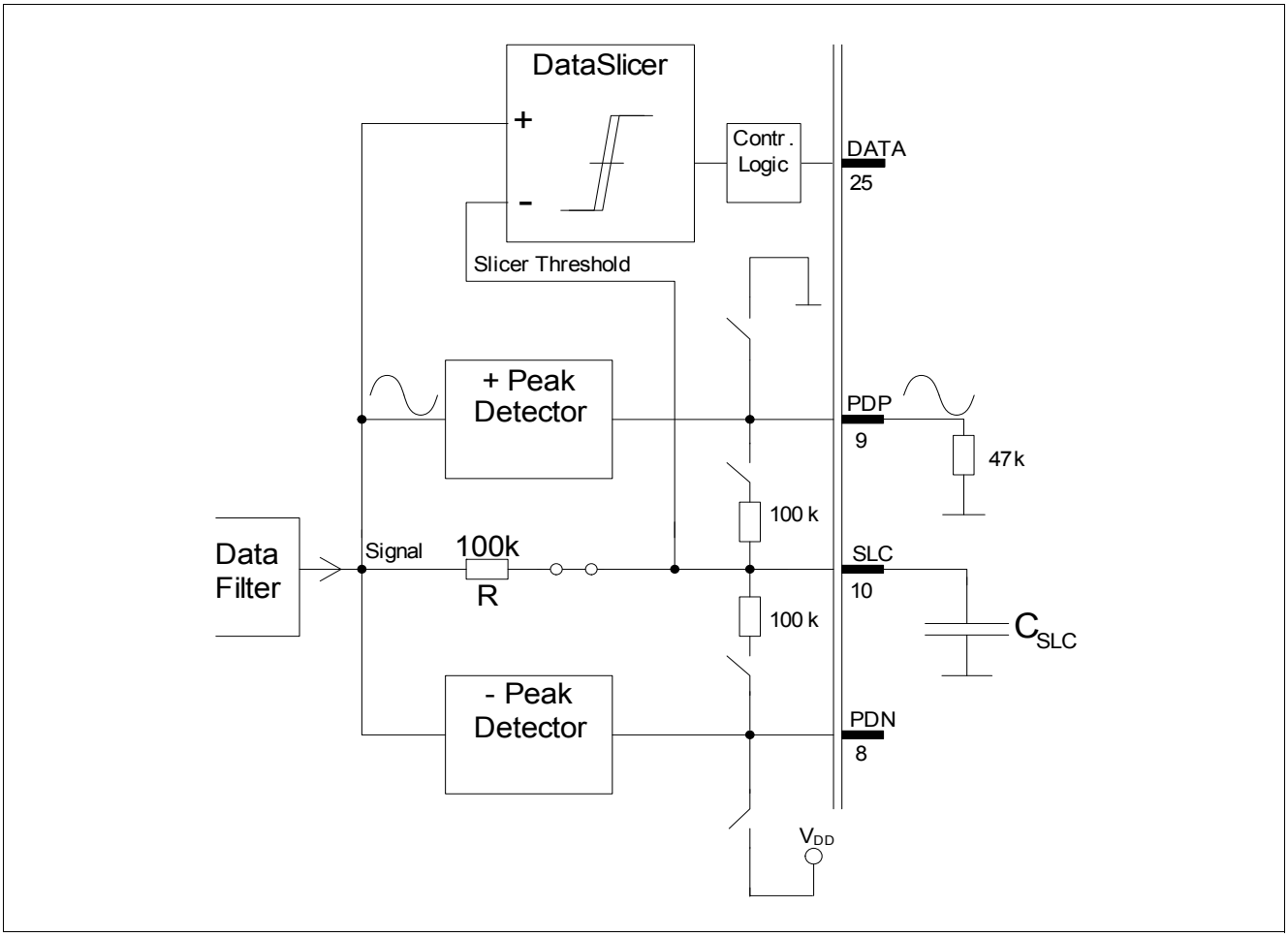


Figure 46 Peak Detector as analog Buffer (v = 1)

3.6.4 Peak Detector – Power Down Mode

For a safe and fast threshold value generation the peak detector is turned on by the sequencer circuit (**Chapter 2.4.18**) only after the entire receiving path is active.

In the off state the output of the positive peak detector is tied down to GND and the output of the negative peak detector is pulled up to V_{CC}.

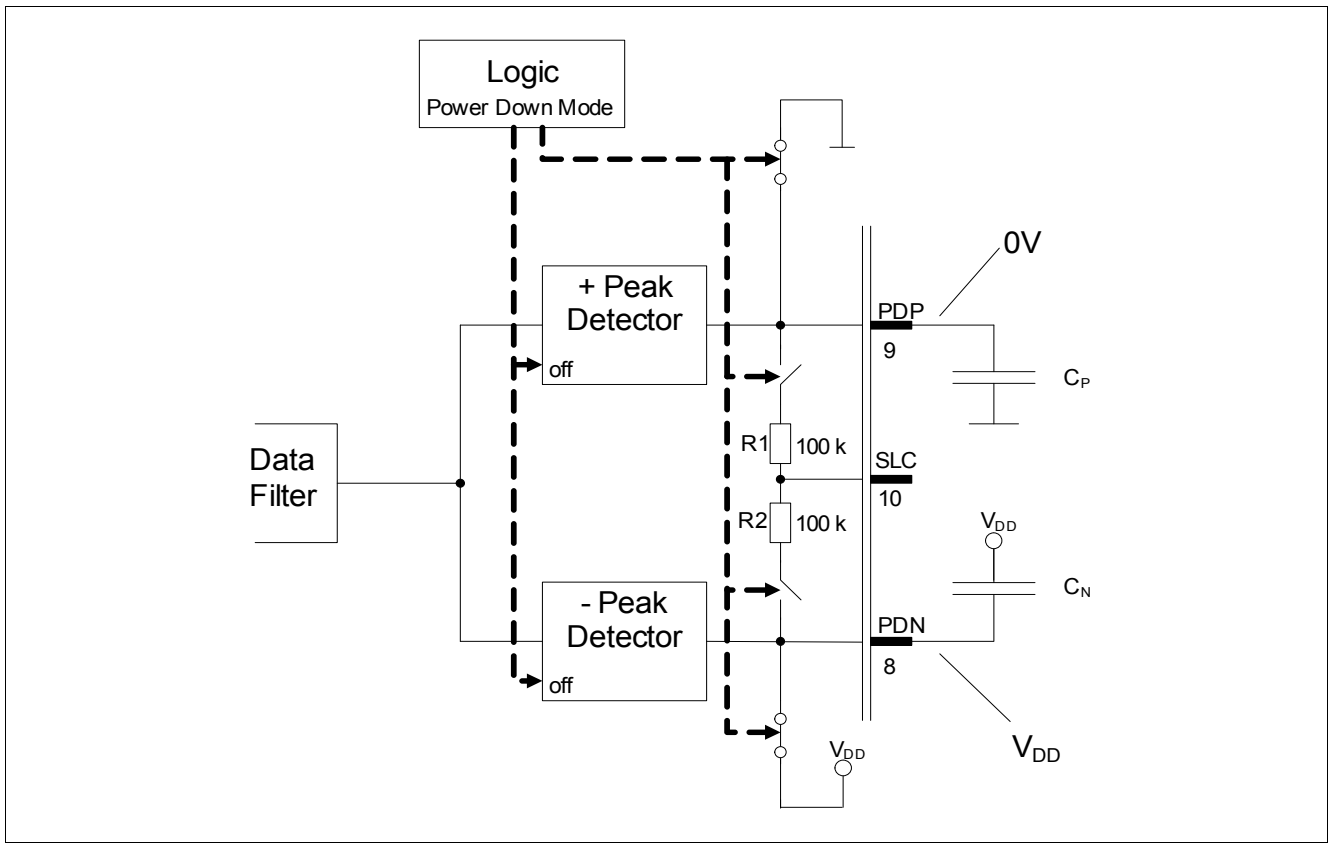


Figure 47 Peak Detector - Power Down Mode

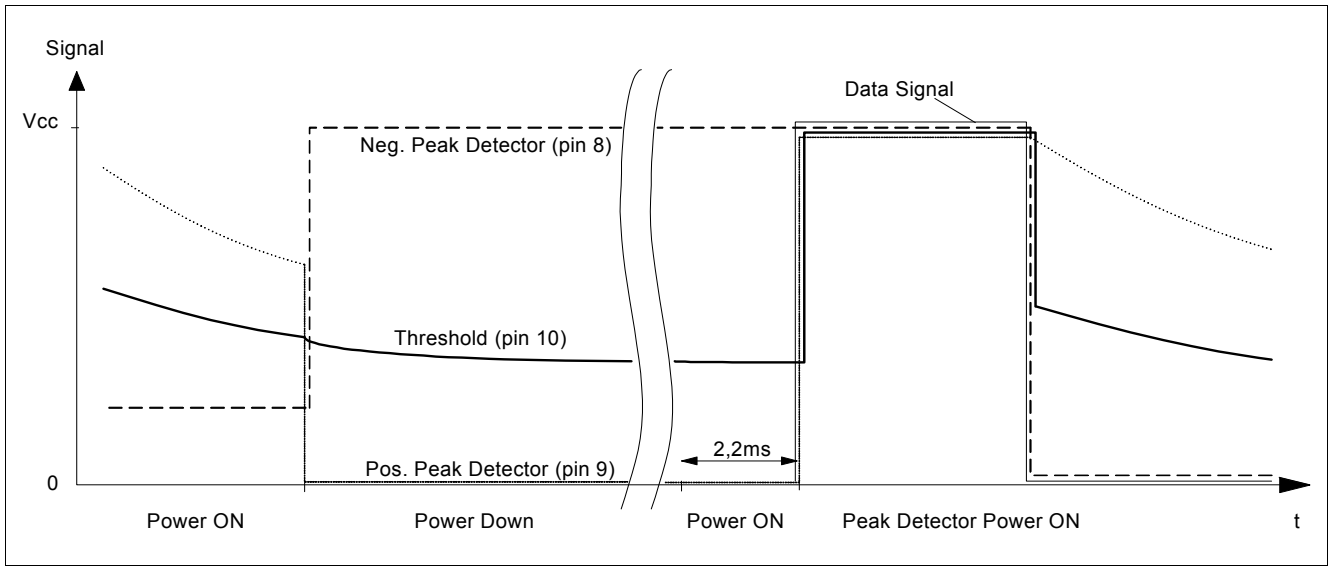


Figure 48 Power Down Mode

3.7 Data Valid Detection

In order to detect valid data two criteria must be fulfilled.

One criteria is the data rate, which can be set in register 06h and 07h. The other one is the received RF power level, which can be set in register 08h in form of the RSSI threshold voltage. Thus for using the data valid detection FSK modulation is recommended.

Timing for data detection looks like the following. Two settings are possible: „Continuous“ and „Single Shot“, which can be set by D5 and D6 in register 00H.

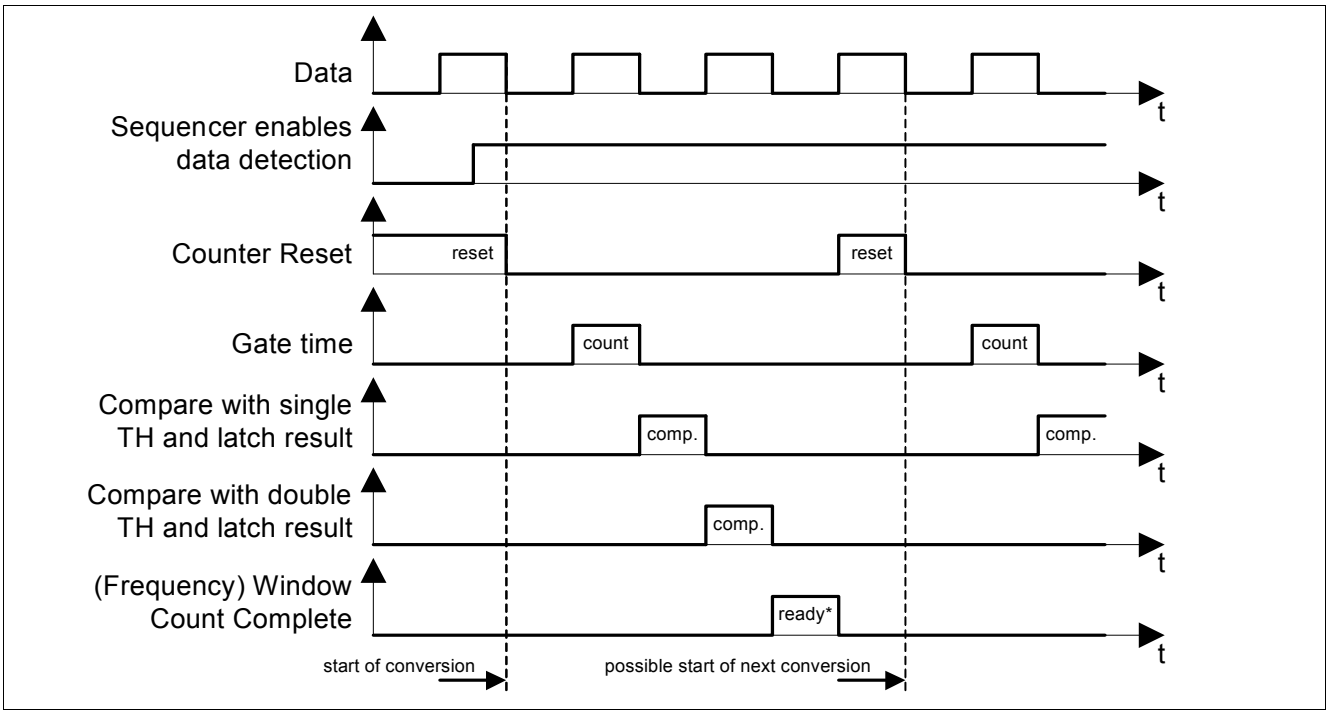


Figure 49 Frequency Detection Timing in Continuous Mode

Note:

1. *Chip internal signal „Sequencer enables data detection“ has a LOW to HIGH transition about 2.6 ms after RX is activated (see **Figure 17**).*
2. *The positive edge of the „Window Count Complete“ signal latches the result of comparison of the analog to digital converted RSSI voltage with TH3 (register 08H). A logic combination of this output and the result of the comparison with single/double TH_x defines the internal signal „data_valid“.*

Figure 49 shows that the logic is ready for the next conversion after 3 periods of the data signal.

Timing in Single Shot mode can be seen in the subsequent figure:

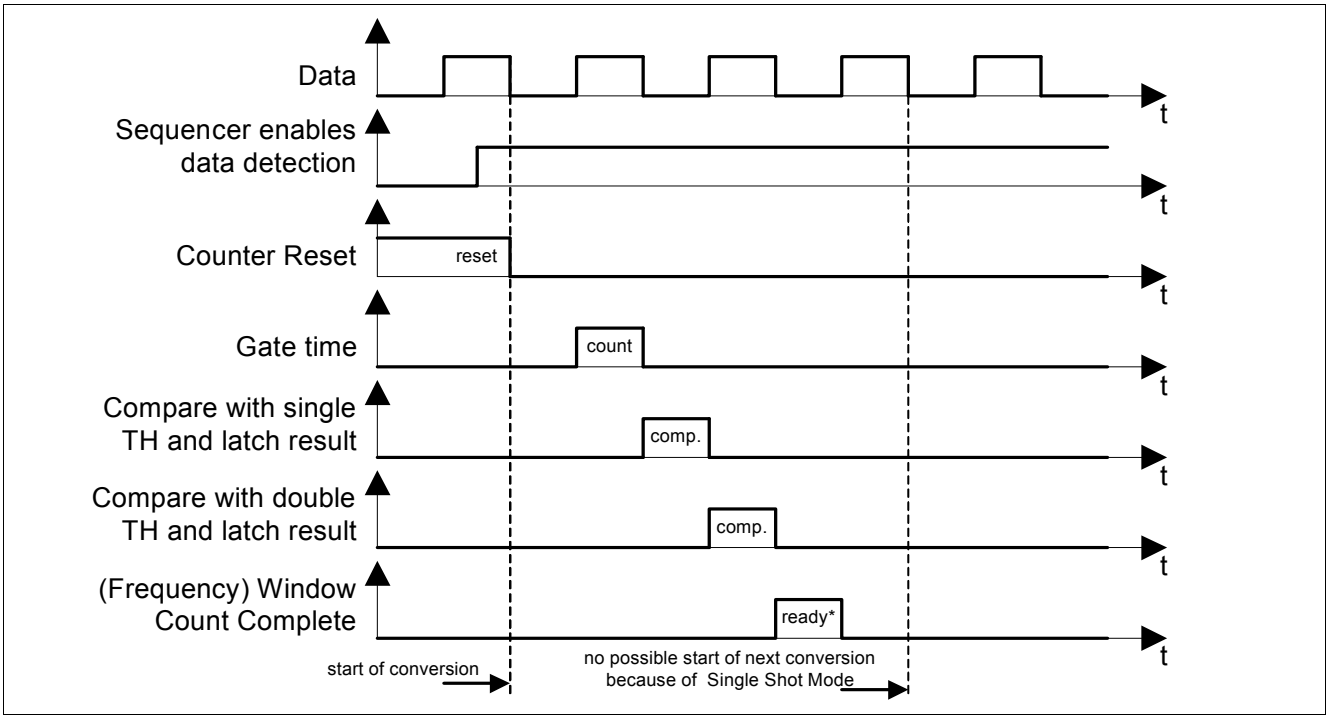


Figure 50 Frequency Detection Timing in Single Shot Mode

3.7.1 Frequency Window for Data Rate Detection

The high time of data is used to measure the frequency of the data signal. For Manchester coding either the data frequency or half of the data frequency have to be detected corresponding to one high time or twice the high time of data signal.

A time period of 3*2*T is necessary to decide about valid or invalid data.

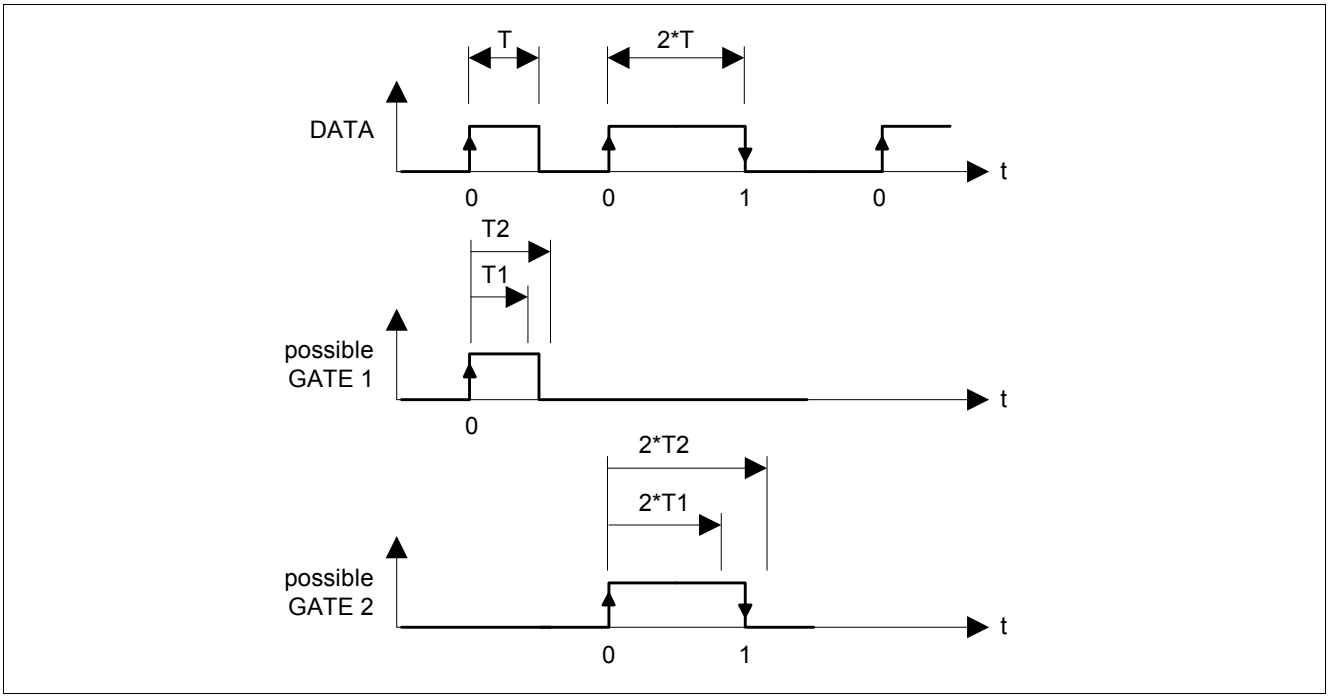


Figure 51 Window Counter Timing

Example to calculate the Thresholds for a given Data Rate

- Data signal Manchester coded
- Data Rate: 2 kbit/s
- f_{clk} = 18,089583 MHz

Then the period equals to

$$2 \cdot T = \frac{1}{2kbit/s} = 0{,}5ms \tag{39}$$

respectively the high time is 0,25 ms.

We set the thresholds to +-10% and get: T1 = 0,225 ms and T2 = 0,275 ms

The thresholds TH1 and TH2 are calculated with following formulas

$$TH1 = T1 \cdot \frac{f_{clk}}{4} \tag{40}$$

$$TH2 = T2 \cdot \frac{f_{clk}}{4} \tag{41}$$

This Yields the following Results

TH1~ 1017 = 001111111001_b

TH2~ 1243 = 010011011011_b

which have to be programmed into the **D0** to **D11** bits of the **COUNT_TH1** and **COUNT_TH2** registers (sub-addresses 06H and 07H), respectively.

Default Values (window counter inactive)

TH1 = 000000000000_b

TH2 = 000000000001_b

Note: The timing window of +/-10% of a given high time T in general does not correspond to a frequency window +/-10% of the calculated data frequency.

3.7.2 RSSI Threshold Voltage - RF Input Power

The RF input power level is corresponding to a certain RSSI voltage, which can be seen in **Chapter 3.5**. The threshold TH3 of this RSSI voltage can be calculated with the following formula:

$$TH3 = \frac{desired\ RSSI\ threshold\ voltage}{1.2V} \cdot (2^6 - 1) \tag{42}$$

As an example a desired RSSI threshold voltage of 500 mV results in TH3~26 = 011010_b, which has to be written into D0 to D5 of the RSSI_TH3 register (sub address 08H).

Default Value (RSSI detection inactive)

TH3 = 111111_b

3.8 Calculation of ON_TIME and OFF_TIME

$$ON = (2^{16}-1) - (f_{RC} * t_{ON}) \quad (43)$$

$$OFF = (2^{16}-1) - (f_{RC} * t_{OFF}) \quad (44)$$

fRC = Frequency of internal RC-Oscillator

Example: t_{ON} = 0,005 s, t_{OFF} = 0,055s, f_{RC} = 32300 Hz

ON = 65535-(32300*0,005) ~ 65373 = 1111111101011101_b

OFF = 65535-(32300*0,055) ~ 63758 = 1111100100001110_b

The values have to be written into the D0 to D15 bits of the ON_TIME and OFF_TIME registers (sub-addresses 04H and 05H).

Default Values

ON = 65215 = 1111111011000000_b

OFF = 62335 = 1111001110000000_b

t_{ON} ~10 ms @ f_{RC} = 32 kHz

t_{OFF} ~100 ms @ f_{RC} = 32 kHz

3.9 Example for Self Polling Mode

The settings for Self Polling Mode depend very much on the timing of the transmitted Signal. To create an example we consider following data structure transmitted in FSK.

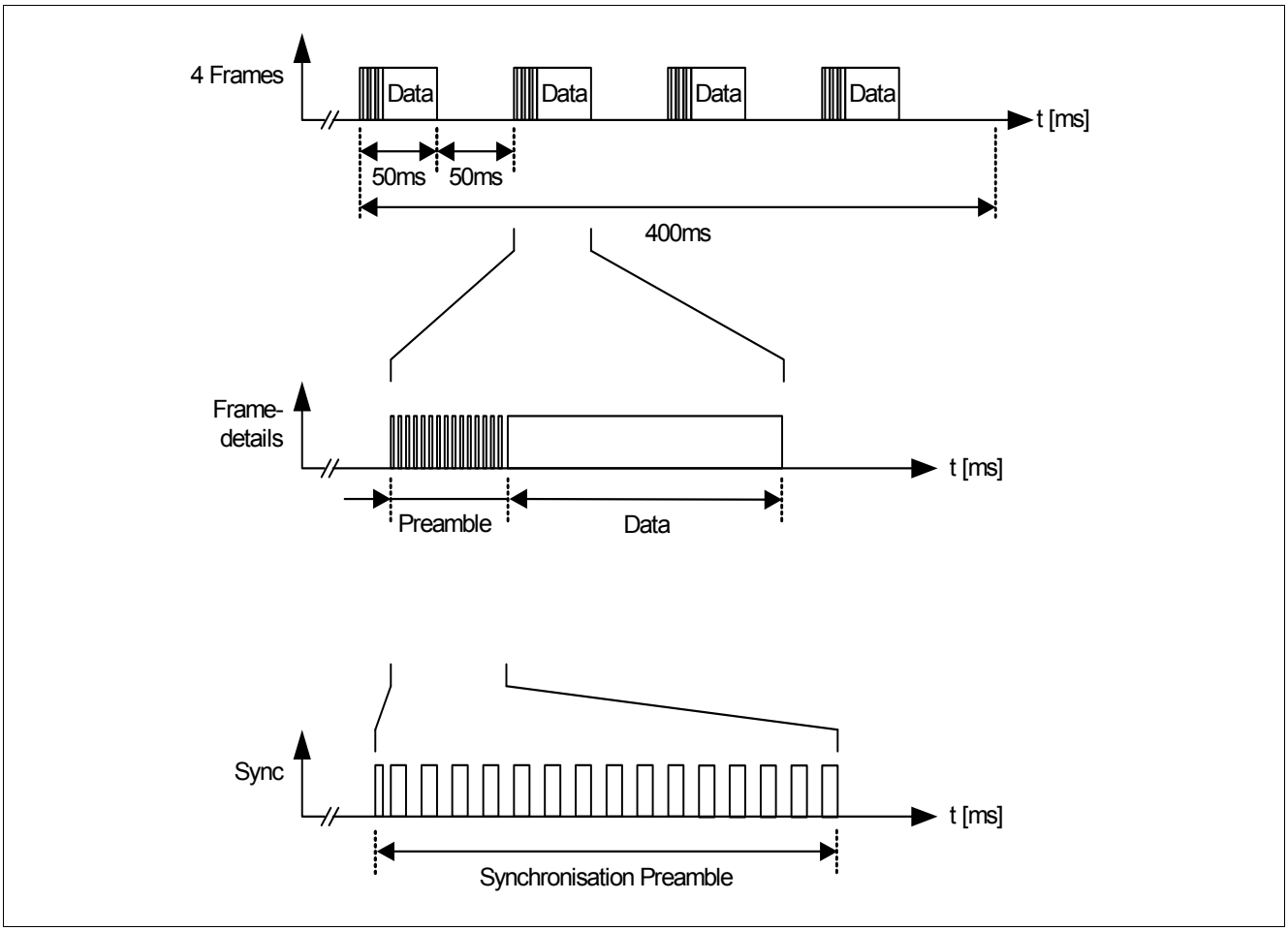


Figure 52 Example for transmitted Data-Structure

According to existing synchronization techniques there are some synchronization bursts in front of the data added (code violation!). A minimum of 4 Frames is transmitted. Data are preferably Manchester encoded to get fastest respond out of the Data Rate Detection.

Target Application

- Received Signal has code violation as described before
- Total mean current consumption below 1 mA
- Data reception within max. 400 ms after first transmitted frame

One possible Solution

t_{ON} = 15 ms, t_{OFF} = 135 ms

This gives 15 ms ON time of a total period of 150 ms which results in max. 0.9 mA mean current consumption in Self Polling Mode. The resulting worst case timing is shown in the following figure:

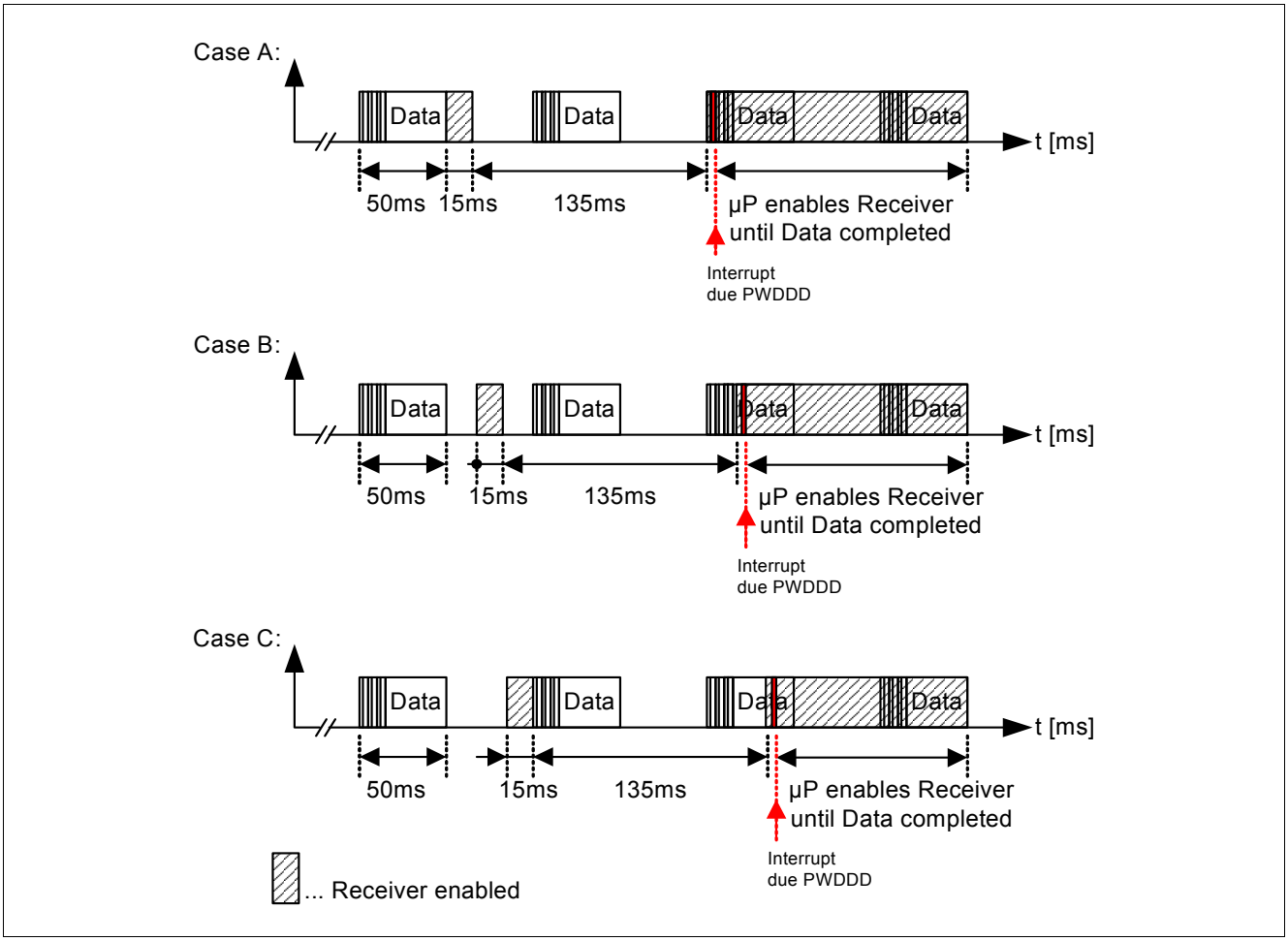


Figure 53 3 Possible Timings

Description

Assumption: the ON time comes right after the first frame (Case A). If OFF time is 135 ms the receiver turns on during Sync-pulses and the PWDDD- pulse wakes up the µP.

If the ON time is in the center of the 50 ms gap of transmission (Case B), the Data Detect Logic will wake up the µP 135 ms later.

If ON time is over just before Sync-pulses (Case C), next ON time is during Data transmission and Data Detect Logic will trigger a PWDDD- pulse to wake up the µP.

*Note: In this example it is recommended to use the Peak Detector for slicer threshold generation, because of its fast attack and slow release characteristic. To overcome the data zero gap of 50 ms larger external capacitors than noted in **Chapter 4.4** at pin12 and 13 are recommended. Further information on calculating these components can be taken from **Chapter 3.6.2**.*

3.10 Default Setup

Default setup is hard wired on chip and effective after a reset or return of power supply.

Table 34 Default Setup

Parameter	Value	IFX-Board	Comment
IQ-Filter Bandwidth	150 kHz		
Data Filter Bandwidth	7 kHz		
Limiter lower fg	470 Hz	47 nF	
Slicing Level Generation	RC	10 nF	
Nom. Frequency Capacity intern (ASK TX, FSK RX)	4.5 pF	434.16 MHz	
FSK_High Frequency Capacity intern (FSK_High, ASK RX)	2.5 pF	+35 kHz	
FSK_Low Frequency Capacity intern (FSK_Low)	1.5 pF	-35 kHz	
LNA Gain	HIGH		
Power Amplifier	HIGH	+10 dBm	
RSSI accuracy settling time	2.6 ms	2.2 nF	
ADC measurement	RSSI		
ON-Time	10 ms		
OFF-Time	100 ms		
Clock out RX PowerON	1 MHz		
Clock out TX PowerON	1 MHz		
Clock out RX PowerDOWN	-		
Clock out TX PowerDOWN	-		
XTAL modulation switch	Bipolar		
XTAL modulation shaping	Off		
RX/TX	-	Jumper	
ASK/FSK	-	Jumper	
PWDDD	PWDN	Jumper removed	
Operating Mode	Slave		

4 Reference Data

4.1 Electrical Data

4.1.1 Absolute Maximum Ratings

Table 35 WARNING

	TDA7255V is intended for use in general electronic equipment (AV equipment, telecommunication equipment, home appliances, amusement equipment, computer equipment, personal equipment, office equipment, measurement equipment) under a normal operation and use condition. Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

Table 36 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply Voltage	V_{CC}/V_{DD}	-0.3		5.8	V		■	1.1
Junction Temperature	T_j	-40		+125	°C		■	1.2
Storage Temperature	T_s	-40		+125	°C		■	1.3
Thermal Resistance	R_{thJA}		50 30		K/W	die pad not soldered, no vias die pad soldered, and vias	■	1.4
ESD HBM integrity (all pins)	$V_{ESD-HBM}$	-1.0		+1.0	kV	AEC Q100-002 EIA/JESD22-A114	■	1.5

4.1.2 Operating Range

Within the operational range the IC operates as explained in the circuit description.

Table 37 Operating Range

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply voltage	V_{CC}/V_{DD}	2.1		5.5	V		■	2.1
Ambient temperature	T_A	-40		+85	°C		■	2.2

Table 37 Operating Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Receive frequency	f_{RX}	433		435	MHz		■	2.3
Transmit frequency	f_{TX}	433		435	MHz		■	2.4

4.1.3 AC/DC Characteristics

AC/DC characteristics involve the spread of values guaranteed within the specified voltage and ambient temperature range. Typical characteristics are the median of the production.

Table 38 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 2.1 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
RECEIVER Characteristics								
Supply current RX FSK	I_{RX_FSK}		9		mA	3 V, FSK, Default		3.1
Supply current RX FSK	I_{RX_FSK}		9.5		mA	5 V, FSK, Default		3.2
Supply current RX ASK	I_{RX_ASK}		8.6		mA	3 V, ASK, Default		3.3
Supply current RX ASK	I_{RX_ASK}		9.1		mA	5 V, ASK, Default		3.4
Sensitivity FSK 10^{-3} BER	RFsens		-115		dBm	FSK @ 35 kHz, 4 kBit/s Manch. Data, Default 5 kHz datafilter, 50 kHz IQ filter	■	3.5
Sensitivity ASK 10^{-3} BER	RFsens		-112		dBm	ASK, 4 kBit/s Manch. data, Default setup 5 kHz datafilter, 50 kHz IQ filter	■	3.6
Input reflection coefficient (S11) f_{RF} = 868 MHz	S11		0.958 / -20 deg					3.7
Power down current	I_{PWDN_RX}		5		nA	5.5 V, all power down		3.8
System setup time (1st power on or reset)	t_{SYSSU}	4	8	12	ms			3.9
Clock Out setup time	t_{CLKSU}		0.5		ms	Stable CLKDIV output signal		3.10
Receiver setup time	t_{RXSU}	1.54	2.2	2.86	ms	DATA out (valid or invalid)		3.11
Data detection setup time	t_{DDSU}	1.82	2.6	3.38	ms	Begin of Data detection		3.12
RSSI stable time	t_{RSSI}	1.82	2.6	3.38	ms	RFin -100 dBm see Chapter 4.5		3.13
Data valid time	t_{Data_Valid}		3.35		ms	4 kBit/s Manch. detected (valid)		3.14
Input P_{1dB}, high gain	P_{1dB}		-63dBm		dBm	3 V, Default, high gain	■	3.15
Input P_{1dB}, low gain	P_{1dB_low}		-42dBm		dBm	3 V, Default, low gain	■	3.16
Selectivity	VBL_1MHz		-55		dB	f_{RF}+/-1 MHz, Default, RFsens+3 dB	■	3.17
LO leakage	P_{LO}		-108		dBm	578,9 MHz	■	3.18
TRANSMITTER Characteristics								
Supply current TX, FSK	I_{TX}		10,7		mA	2.1 V, high power		3.19

Table 38 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 2.1 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Supply current TX, FSK	I_{TX}		13,5		mA	3 V, high power		3.20
Supply current TX, FSK	I_{TX}		18,3		mA	5 V, high power		3.21
Output power	P_{out}		+6		dBm	2.1 V, high power	■	3.22
Output power	P_{out}		9		dBm	3 V, high power	■	3.23
Output power	P_{out}		13		dBm	5 V, high power	■	3.24
Supply current TX, FSK	I_{TX}		5		mA	2.1 V, low power		3.25
Supply current TX, FSK	I_{TX}		7.5		mA	3 V, low power		3.26
Supply current TX, FSK	I_{TX}		15		mA	5 V, low power		3.27
Output power	P_{out_low}		-32		dBm	2.1 V, low power	■	3.28
Output power	P_{out_low}		-1		dBm	3 V, low power	■	3.29
Output power	P_{out_low}		11		dBm	5 V, low power	■	3.30
Power down current	I_{PWDN_TX}		5		nA	5.5 V, all power down		3.31
Clock-Out setup time	t_{CLKSU}		0.5		ms	Stable CLKDIV output signal		3.32
Transmitter setup time	t_{TXSU}	0.77	1.1	1.43	ms	PWDN-->PON or RX-->TX	■	3.33
Spurious f_{RF}+/-f_{clock}	P_{clock}		-59		dBm	3 V, 50 Ω Board, Default (1 MHz)	■	3.34
Spurious f_{RF}+/-f_{XTAL}	P_{1st}		-74		dBm	3 V, 50 Ω Board	■	3.35
Spurious 2nd harmonic	P_{2nd}		-43		dBm	3 V, 50 Ω Board	■	3.36
Spurious 3rd harmonic	P_{3rd}		-43		dBm	3 V, 50 Ω Board	■	3.37

1: including pin diode current (RX/TX-switch)

130 uA @ 2.1 V; 310 uA @ 3 V; 720 uA @ 5 V

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

Table 39 AC/DC Characteristics with T_{AMB} = 25 °C, V_{CC} = 2.1 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
GENERAL Characteristics								
Power down current timer mode (standby)	I_{PWDN_32k}		9		uA	3 V, 32 kHz clock on		4.1
Power down current timer mode (standby)	I_{PWDN_32k}		11		uA	5 V, 32 kHz clock on		4.2
Power down current with XTAL ON	I_{PWDN_Xtl}		750		uA	3 V, CONFIG9 = 1		4.3
Power down current with XTAL ON	I_{PWDN_Xtl}		860		uA	5 V, CONFIG9 = 1		4.4
32 kHz oscillator freq.	$f_{32\ kHz}$	24	32	40	kHz			4.5
XTAL startup time	t_{XTAL}		0.3		ms	IFX Board with Crystal Q1 as specified in Chapter 4.4	■	4.6
Load capacitance	C_{C0max}		5		pF		■	4.7
Serial resistance of the crystal	R_{max}			100	Ω		■	4.8
Input inductance XOUT	L_{OSC}		2.7		uH	With pad on evaluation board	■	4.9
Input inductance XOUT	L_{OSC}		2.45		uH	Without pad on evaluation board	■	4.10
FSK demodulator gain	G_{FSK}		2.4		mV/kHz			4.11
RSSI @ -120 dBm	$U_{-120\ dBm}$		0.4		V	Default setup	■	4.12
RSS I@ -100 dBm	$U_{-100\ dBm}$		0.6		V	Default setup	■	4.13
RSSI @ -70 dBm	$U_{-70\ dBm}$		0.96		V	Default setup	■	4.14
RSSI @ -50 dBm	$U_{-50\ dBm}$		1.1		V	Default setup	■	4.15
RSSI Gradient	G_{RSSI}		12		mV/dB	Default setup	■	4.16
IQ-Filter bandwidth	f_{3dB_IQ}	115	150	185	kHz	Default setup	■	4.17
Data-Filter bandwidth	f_{3dB_LP}	5.3	7	8.7	kHz	Default setup	■	4.18
V_{CC}-V_{tune} RX, Pin3	$V_{cc\text{-}tune,RX}$	0.5	1	1.6	V	f_{Ref} = 18.08956 MHz		4.19
V_{CC}-V_{tune} TX, Pin3	$V_{cc\text{-}tune,TX}$	0.5	1.1	1.6	V	f_{Ref} = 18.08956 MHz		4.20

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.1.4 Digital Characteristics

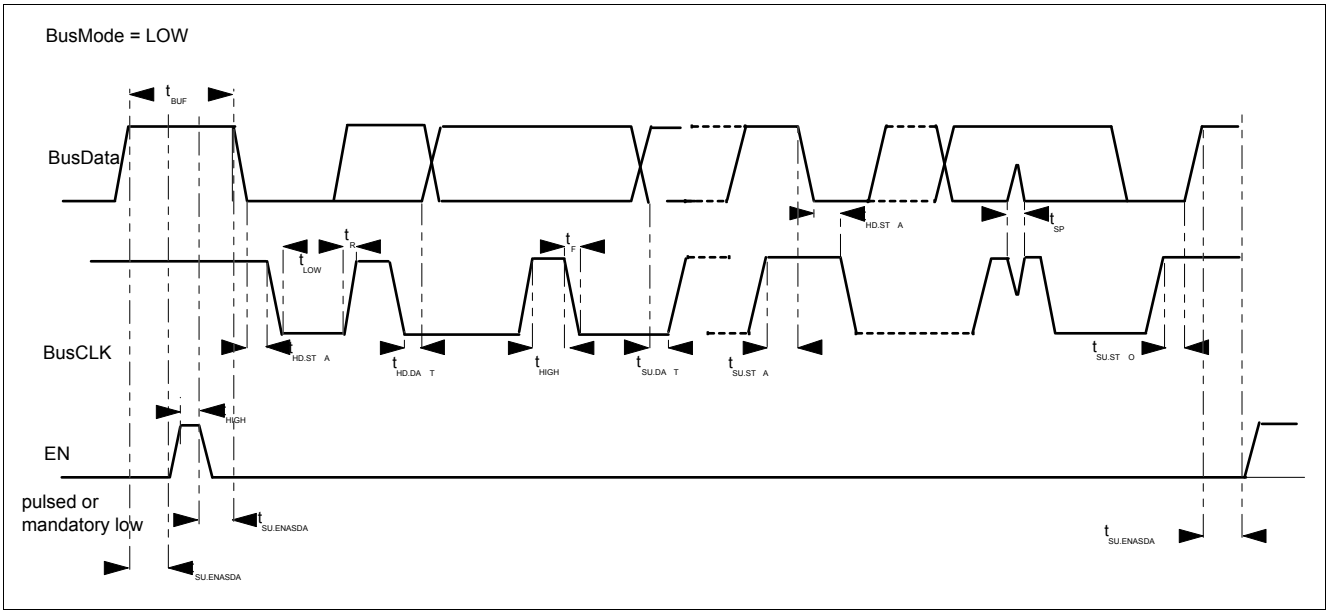


Figure 54 I²C Bus Timing

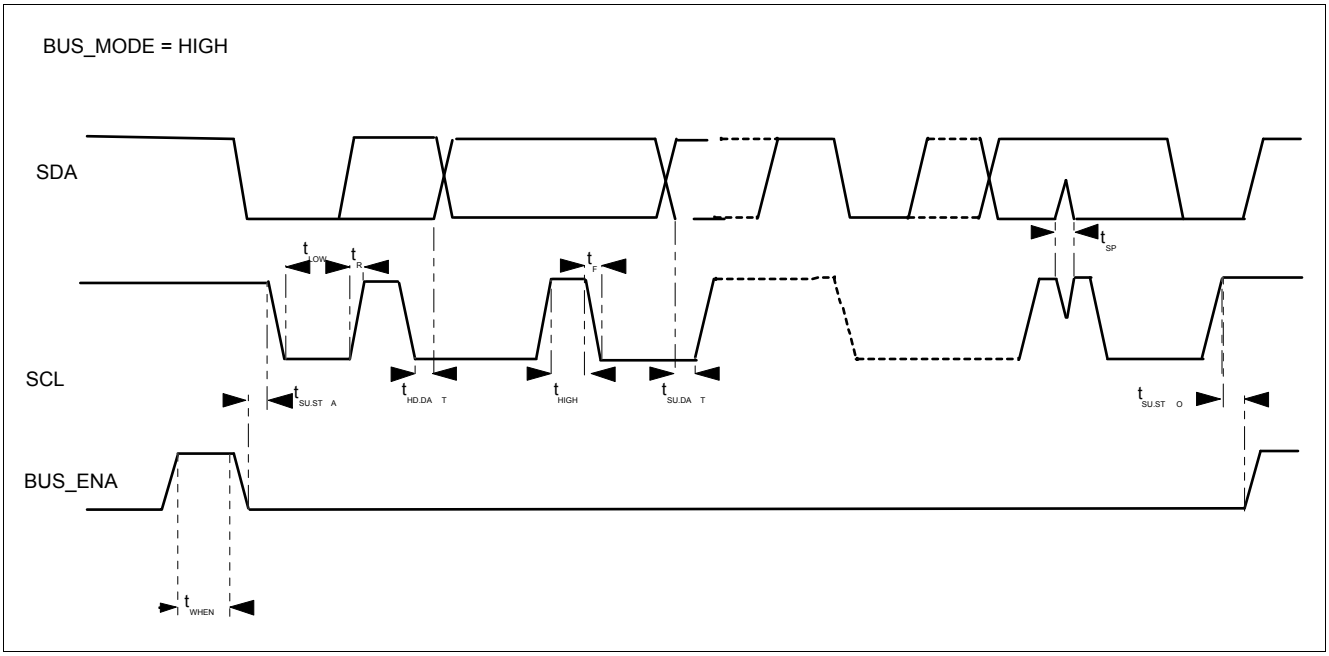


Figure 55 3-Wire Bus Timing

Table 40 Digital Characteristics with T_{AMB} = 25 °C, V_{DD} = 2.1 ... 5.5 V

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Data rate TX ASK[1)]	$f_{TX.ASK}$		10	100	kBaud	PRBS9, Manch. @+9 dBm	■	5.1
Data rate TX FSK[1)]	$f_{TX.FSK}$		10	32	kBaud	PRBS9, Manch. @+9 dBm @35 kHz dev.	■	5.2
Data rate RX ASK	$f_{RX.ASK}$		10	50	kBaud	PRBS9, Manch.	■	5.3
Data rate RX FSK	$f_{RX.FSK}$		10	64	kBaud	PRBS9, Manch. @100 kHz dev.	■	5.4
Data rate RX FSK	$f_{RX.FSK}$		10	28.8	kBaud	PRBS9, Manch. @35 kHz dev.	■	5.5
Digital inputs High-level input voltage Low-level input voltage	 V_{IH} V_{IL}	 V_{DD}-0.2 0		 V_{DD} 0.2	 V V		■	5.6
RXTX Pin 5 TX operation int. controlled	V_{OL}		0.4 1.15		V V	@V_{DD} = 3 V Isink = 800 uA Isink = 3 mA	■	5.7
CLKDIV Pin 26 t_{rise} (0.1*$V_{DD}$to 0.9*V_{DD}) t_{fall} (0.9*V_{DD} to 0.1*V_{DD}) Output High Voltage Output Low Voltage	 t_r t_f V_{OH} V_{OL}		 35 30 V_{DD}-0.4 0.4		 ns ns V V	@V_{DD} = 3 V Load 10 pF Load 10 pF Isource = 350 uA Isink = 400 uA	■	5.8
Bus Interface Characteristics								
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	V_{DD} = 5 V	■	5.9
LOW level output voltage at BusData	V_{OL}			0.4	V	3 mA sink current V_{DD} = 5V	■	5.11
SLC clock frequency	f_{SLC}	0		400	kHz	V_{DD}=5 V	■	5.12
Bus free time between STOP and START condition	f_{BUF}	1.3			µs	Only I²C mode V_{DD} = 5 V	■	5.13
Hold time (repeated) START condition.	$t_{HO.STA}$	0.6			µs	After this period, the first clock pulse is generated, only I²C	■	5.14
LOW period of BusCLK clock	t_{LOW}	1.3			µs	V_{DD} = 5 V	■	5.15
HIGH period of BusCLK clock	t_{HIGH}	0.6			µs	V_{DD} = 5 V	■	5.16

Table 40 Digital Characteristics with T_{AMB} = 25 °C, V_{DD} = 2.1 ... 5.5 V (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition	Test	Number
		Min.	Typ.	Max.				
Setup time for a repeated START condition	$t_{SU.STA}$	0.6			µs	Only I²C mode	■	5.17
Data hold time	$t_{HD.DAT}$	0			ns	V_{DD} = 5 V	■	5.18
Data setup time	$t_{SU.DAT}$	100			ns	V_{DD} = 5 V	■	5.19
Rise, fall time of both BusData and BusCLK signals[2)]	t_R, t_F	20+ 0.1C_b		300	ns	V_{DD} = 5 V	■	5.20
Setup time for STOP condition	$t_{SU.STO}$	0.6			µs	Only I²C mode V_{DD} = 5 V	■	5.21
Capacitive load for each bus line	C_b			400	pF	V_{DD} = 5 V	■	5.22
Setup time for BusCLK to EN	$t_{SU.SCLEN}$	0.6			µs	Only 3-wire mode V_{DD} = 5 V	■	5.23
H-pulsewidth (EN)	t_{WHEN}	0.6			µs	V_{DD} = 5 V	■	5.24

1) Limited by transmission channel bandwidth and depending on transmit power level; ETSI regulation EN 300 220 fulfilled, see **Chapter 3.1**

2) C_b = capacitance of one bus line

Attention: Test ■ means that the parameter is not subject to production test. It was verified by design/characterization.

4.2 Test Circuit

The device performance parameters marked with **X** in **Chapter 4.1.3** were measured on an Infineon evaluation board (IFX board).

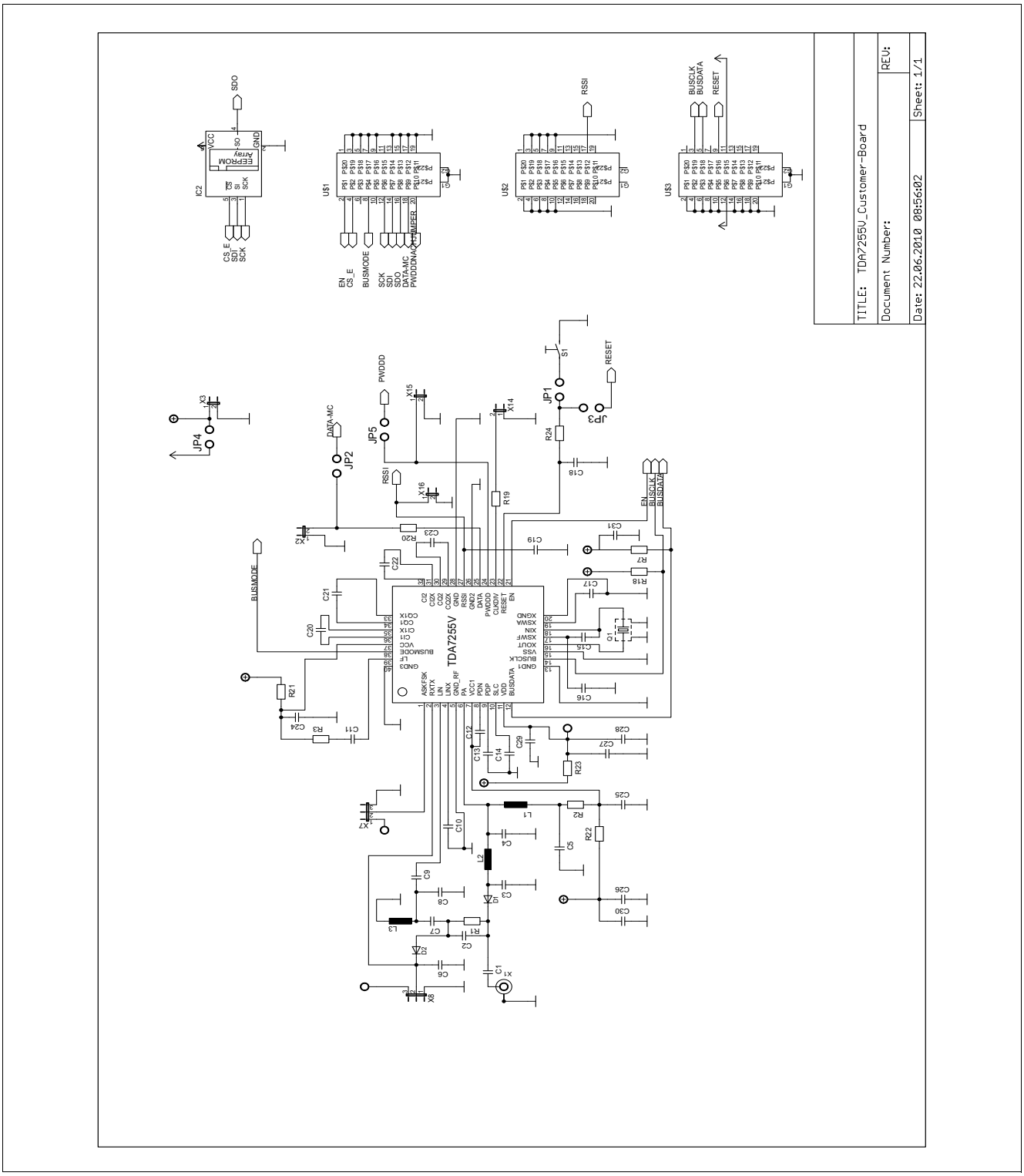


Figure 56 Schematic of the Evaluation Board

4.3 Test Board Layout

Gerber-files for this Testboard are available on request.

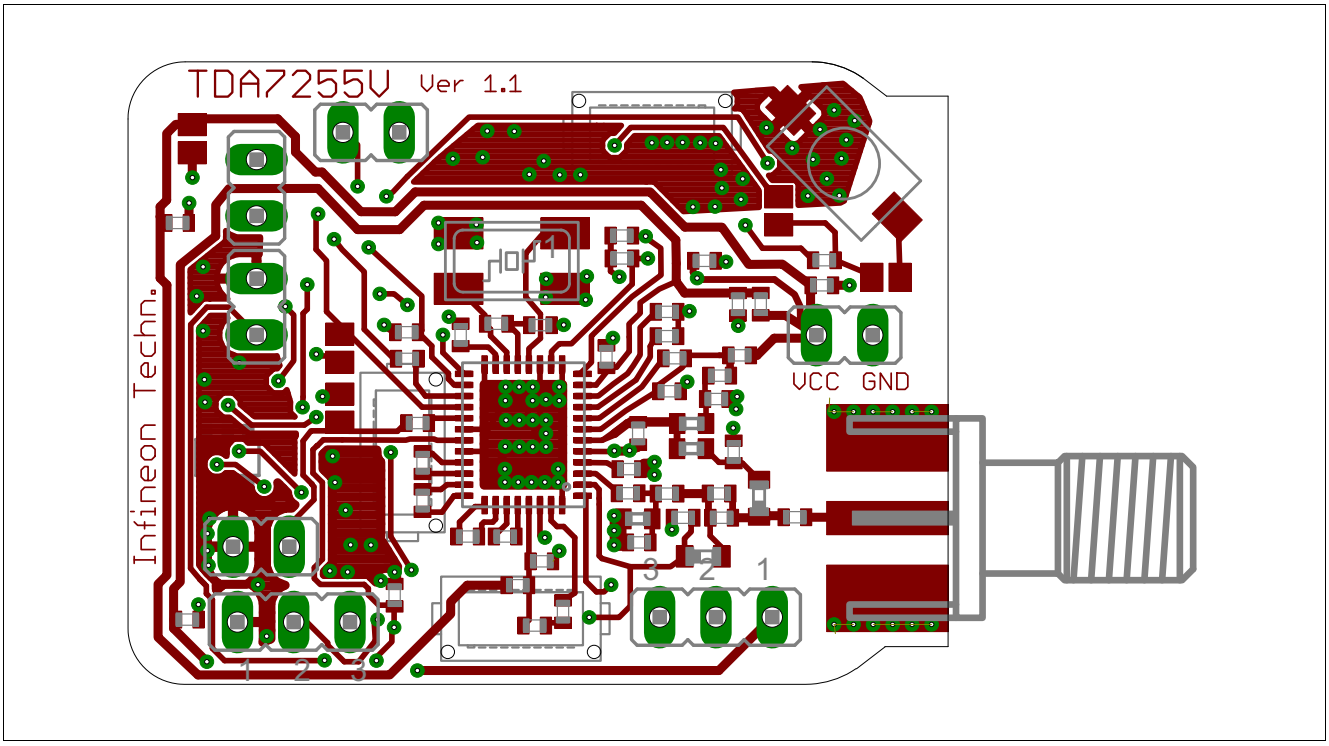


Figure 57 Top Layer of the Customer Board TDA7255V

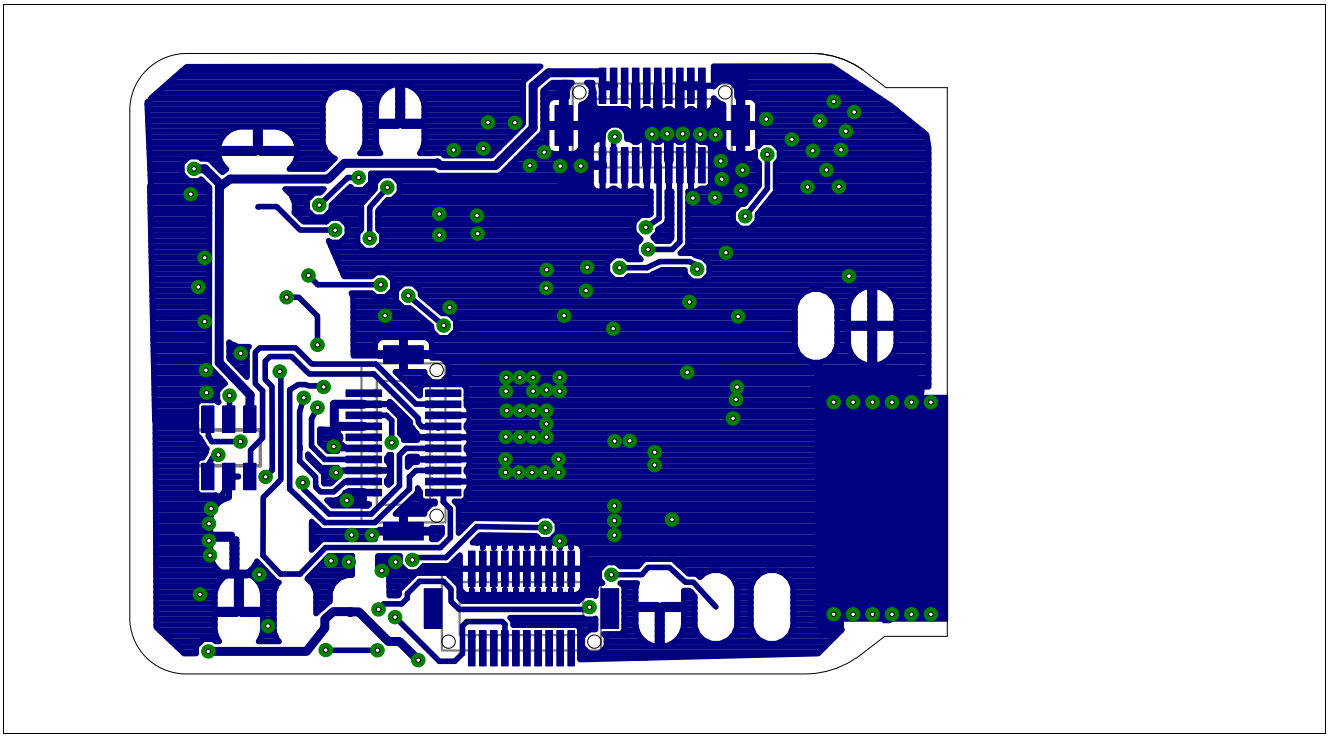


Figure 58 Bottom Layer of the Customer Board TDA7255V

Notes

1. *The LNA and PA matching network was designed for minimum required space and maximum performance and thus via holes were deliberately placed into solder pads.*
   In case of reproduction please bear in mind that this may not be suitable for all automatic soldering processes.
2. *Please keep in mind not to layout the CLKDIV line directly in the neighborhood of the crystal and the associated components.*
3. *Difference in supply voltage especially between pin 1 and pin 15 is recommended to be lower than 30 mV, therefore a serial resistor in the V_{DD} supply line, as mentioned on page 15 and in **Chapter 4.4**, is strongly recommended.*

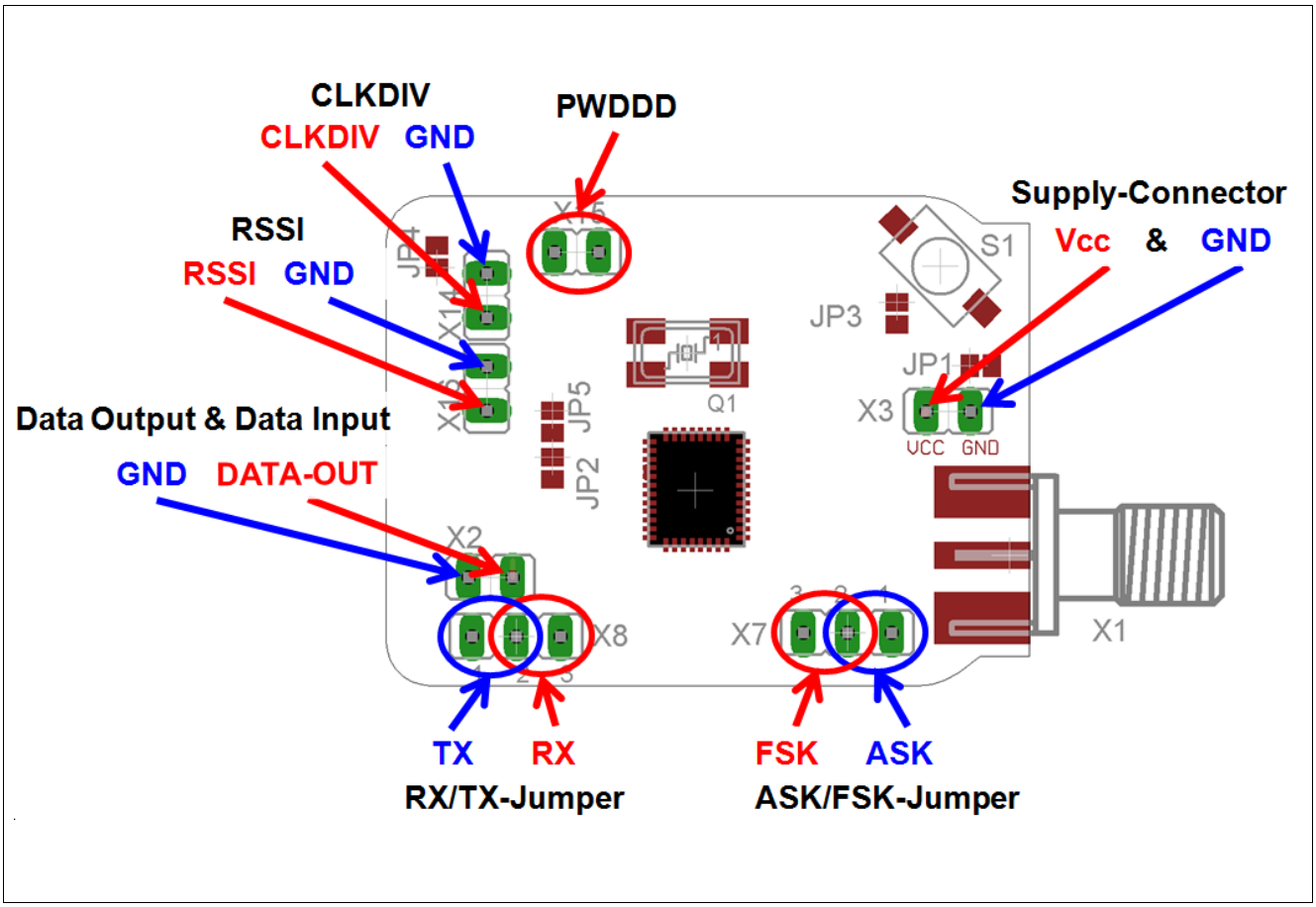


Figure 59 Placement of connectors and jumpers (axial)

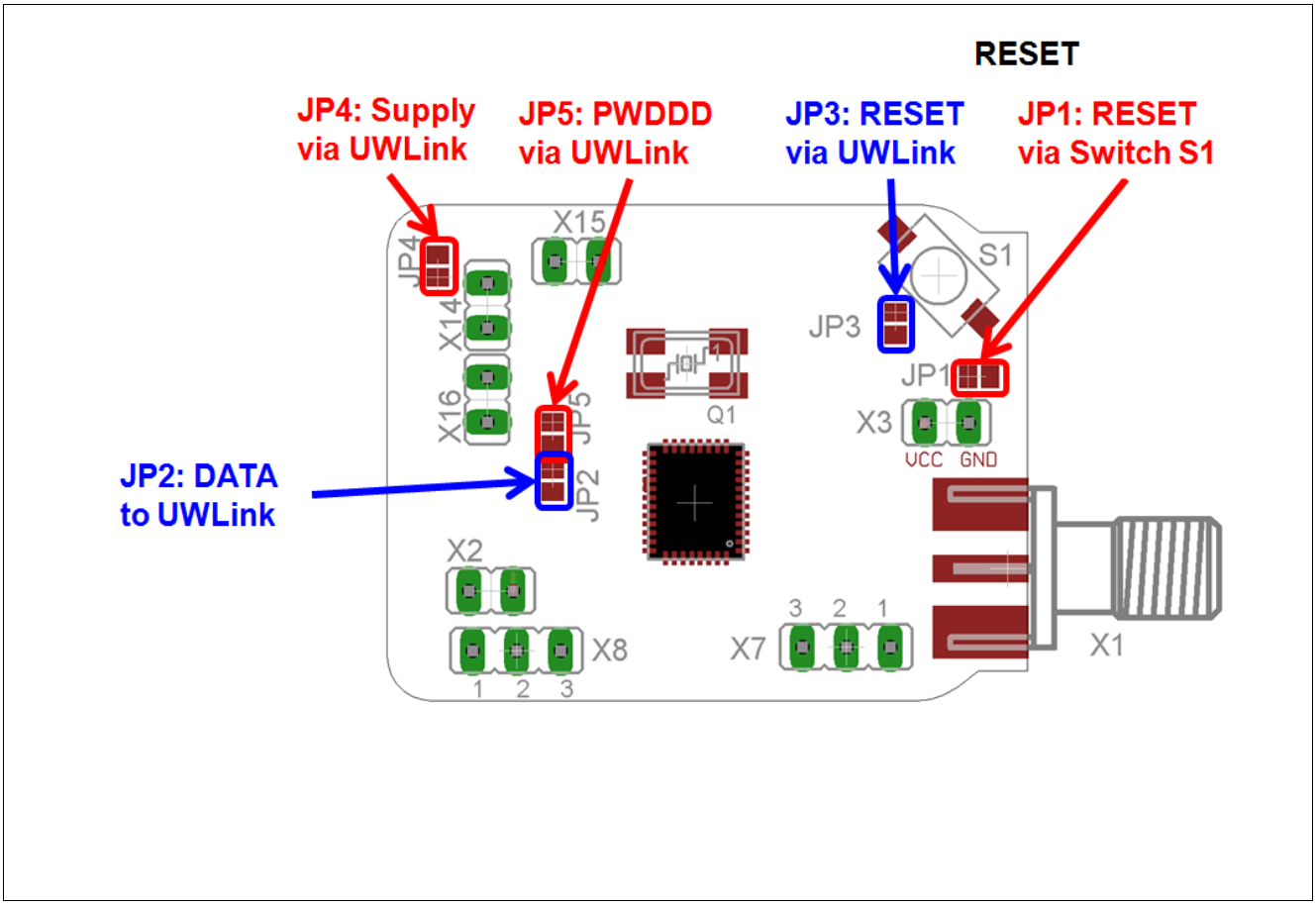


Figure 60 Placement of connectors and jumpers (SMD)

Initially JP2 (Data to UWLink), JP3 (RESET via UWLink), JP4 (Supply via UWLink) and JP5 (PWDDD via UWLink) are open. Closing JP2 enables to apply a PRBS9 data sequence from 200 bit/s up to 80kbit/s to the data input (DATA) in case of transmit mode by the TDA7255V Explorer. Closing JP5 enables to control the PDWDDD-pin via the TDA7255V Explorer. A supply voltage of ~3.3 V for the TDA7255V Extension Board can be provided from the UWLink board when closing JP4. But don't forget to remove the external supply in that case.

Opening JP1 and closing JP3 enables the facility to RESET the TDA7255V by clicking the reset button at the TDA7255V Explorer.

4.4 Bill of Materials

Table 41 Bill of Materials

Reference	Value	Specification	Tolerance
R1	4 k7	0402	+/-5%
R2	0	0402	+/-5%
R3	---	0402	+/-5%
R6	---	0402	+/-5%
R7	4 k7	0402	+/-5%
R18	1 M	0402	+/-5%
R19	560	0402	+/-5%
R20	1 k	0402	+/-5%
R21	0	0402	+/-5%
R22	0	0402	+/-5%
R23	10	0402	+/-5%
R24	180	0402	+/-5%
C1	33 pF	0402	+/-5%
C2	1,8 pF	0402	+/-0,1 pF
C3	27 pF	0402	+/-1%
C4	12 pF	0402	+/-0,1 pF
C5	1 nF	0402	+/-5%
C6	1 nF	0402	+/-5%
C7	10 pF	0402	+/-0,1 pF
C8	---	0402	+/-0,1 pF
C9	27 pF	0402	+/-1%
C10	100 pF	0402	+/-5%
C11	---	0402	+/-5%
C12	10 nF	0402	+/-10%
C13	10 nF	0402	+/-10%
C14	10 nF	0402	+/-10%
C15	12 pF	0402	+/-0,1 pF
C16	3.3 pF	0402	+/-0,1 pF
C17	15 pF	0402	+/-1%
C18	10 nF	0402	+/-10%
C19	2,2 nF	0402	+/-10%
C20	47 nF	0402	+/-10%
C21	47 nF	0402	+/-10%
C22	47nF	0402	+/-10%
C23	47 nF	0402	+/-10%
C24	100 nF	0402	+/-10%

Table 41 Bill of Materials (cont'd)

Reference	Value	Specification	Tolerance
C25	100 nF	0402	+/-10%
C26	100 nF	0402	+/-10%
C27	100 nF	0402	+/-10%
C28	100 nF	0402	+/-10%
C29	100 nF	0402	+/-10%
C30	100 nF	0402	+/-10%
C31	100 nF	0402	+/-10%
L1	100 nH	Coilcraft SIMID 0402HP, + 2%	+/-2%
L2	12 nH	Coilcraft SIMID 0402HP, + 2%	+/-2%
L3	36 nH	Coilcraft SIMID 0402HP, + 2%	+/-2%
IC1	TDA7255V	PG-VQFN-40	
IC2	25AA040AT	EEPROM 4KB (MICROCHIP)	
Q1	18.089583 MHz	Hertz: TSS-6035 Spec.-Nr.: 1053-935	C1 = 8 fF, C0 = 2.1 pF, CL = 20 pF
S1	1-pol. push-button	MULTICOMP MCTAEF-25N-V	
D1, D2	BAR63-02W	SCD-80 (Infineon)	
X1	SMA-socket		
X2, X3, X14, X15, X16	2-pol.	2-pole pin connector 2,54 mm	
X7, X8	3-pol.	3-pole pin connector 2,54 mm	
JP1	Solder bridge	Solder bridge closed	
JP2, JP3, JP4, JP5	Solder bridge	Solder bridge open	
U$1, U$2, U$3	20-pol. connector	Hirose: DF12(3.5)-20DS-0.5 V	

Note: Serial resistors in supply lines (R21, R22, R23) should be equipped as shown in the table above.

w w w . i n f i n e o n . c o m

Published by Infineon Technologies AG