AD9739A-EBZ
Quick Start Guide

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Getting Started with the AD9739A-EBZ Evaluation Board

WHAT'S IN THE BOX

AD9737A or AD9739A-EBZ Evaluation Board
Evaluation Board CD
Mini-USB Cable

RECOMMENDED EQUIPMENT

Low Phase Noise Sinusoidal Signal Generator or ADF4350 Evaluation Board
Spectrum Analyzer
Data Pattern Generator Series 2 (DPG2)

INTRODUCTION

The purpose of this document is to get the AD9737A or AD9739A evaluation board up and running as quickly as possible and provide guidance on how to optimize the controllers in the part to get the optimal performance out of the AD9737A/AD9739A.

SOFTWARE

The AD9737A/AD9739A-EBZ are designed to receive data from a DPG2. The DAC Software Suite, plus the AD9737A/AD9739A Update, is required for evaluation. The DAC Software Suite is included on the Evaluation Board CD, or can be downloaded from the DPG web site at http://www.analog.com/dpg. This will install DPGDownloader (for loading vectors into the DPG2) and the AD9737A or AD9739A SPI application.

HARDWARE SETUP

To operate the board, a power supply capable of +5vdc, 2A should be connected to J17. A spectrum analyzer or an oscilloscope to view the DAC output should be connected to J1. The diagram in Figure 1 shows the location of each connection. A low jitter (< 0.5psec RMS) sine or square wave clock source should be connected to J3. The DC level of the clock is unimportant since the clock is AC-coupled on the evaluation board before the CLKP/N inputs. The included USB cable should be used to connect the Evaluation Board to a PC. Note that the software described above should be installed before connecting the USB cable.

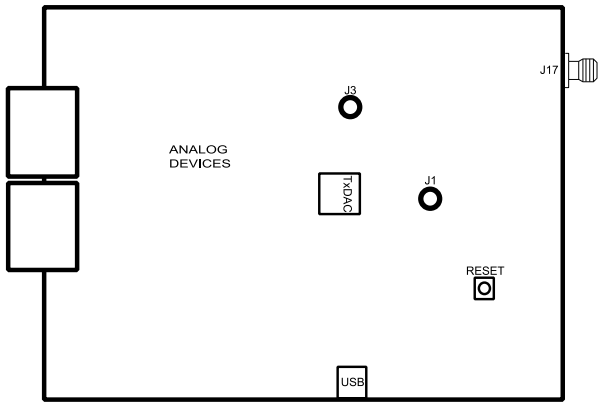

Figure 1

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GETTING STARTED

This quick-start will setup a single-tone output from the AD9737A/AD9739A to provide a brief introduction to the part, as well as a basic functionality test. To begin, open the AD9737A/AD9739A SPI application (Start > Programs > Analog Devices > AD9737A/AD9739A-EBZ > AD9737A/AD9739A SPI). Connect a +5Vdc power supply to J17, and connect a 2GHz, 0dBm clock to J3.

Enable Mu Controller

In order to optimize and lock the Mu Controller, it is only necessary to have the DAC clock running (no data needs to be presented). Click the MU_ENA button in the MU Controller section of the SPI application, as shown in Figure 2. Then run the SPI application by clicking on the Run button ( ) in the upper left of the screen.

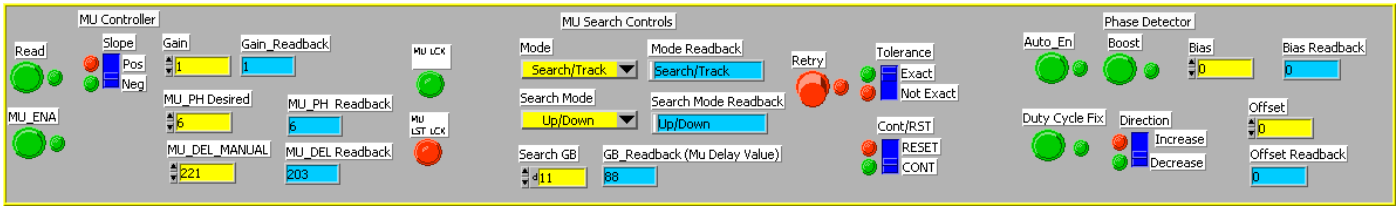

Figure 2

Load Pattern from the DPG2

Open DPGDownloader (Start > Programs > Analog Devices > DPG > DPGDownloader). Ensure that "AD9737A/AD9739A" is selected in the *Evaluation Board* drop-down list. For this evaluation board, "LVDS" is the only valid *Port Configuration*, and will be selected automatically. The *Data Clock Frequency* display should read approximately 500MHz.

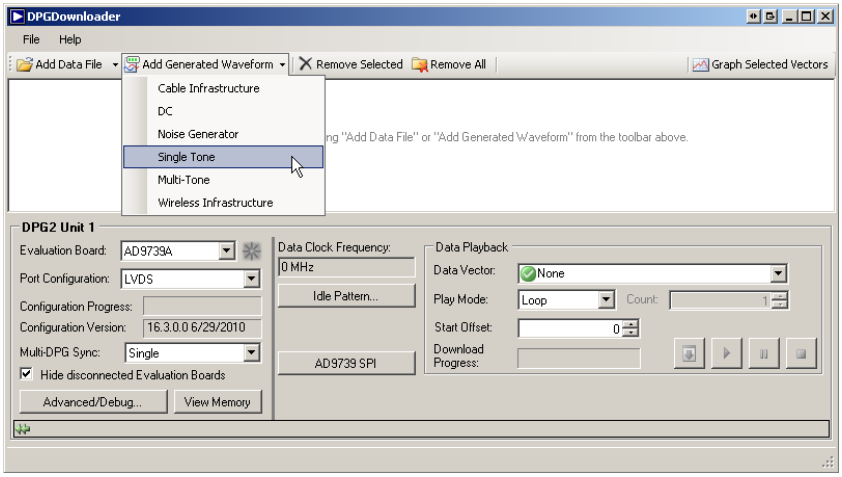

Figure 3

Click on *Add Generated Waveform*, and then *Single Tone*, as shown in Figure 3. A Single Tone panel will be added to the vector list. Start by entering the Clock Frequency (2GHz in this case). You can enter 2G in the box. Next, enter 180MHz (180M) as the desired frequency of the tone. The DAC Resolution should be set at 14 bits.

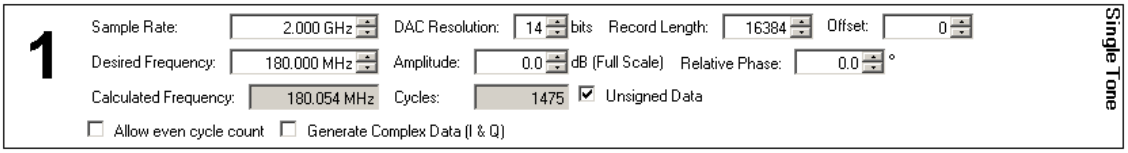

Figure 4

Next, in the lower portion of the screen, select "1: Single Tone" as the Data Vector. The other options can be left at their default.

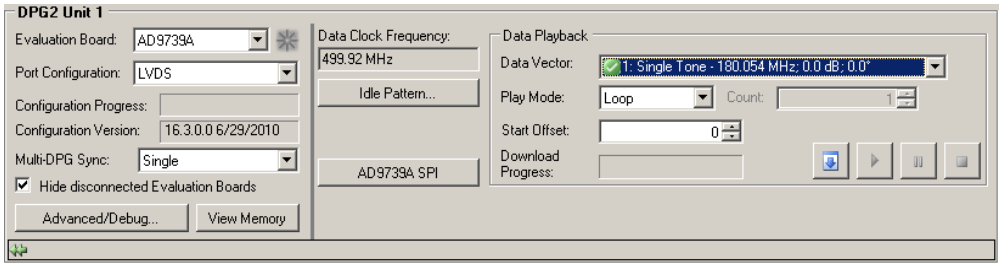

Figure 5

After the DPG2 is correctly setup, click the Download button ( ) in the lower right, then the Play button ( ) to begin vector playback into the AD9737A/AD9739A.

Enable LVDS Controller

Once the pattern is loaded into the DPG2 and running, the final step is to enable the LVDS Controller. In the AD9737A or AD9739A SPI application, enable the *RCV_LOOP* and *RCV_ENA* buttons. Click the Run button ( ). Once the run is complete, the *RCVR LCK* and *RCVR TRX ON* indicators should be green, as shown in Figure 9.

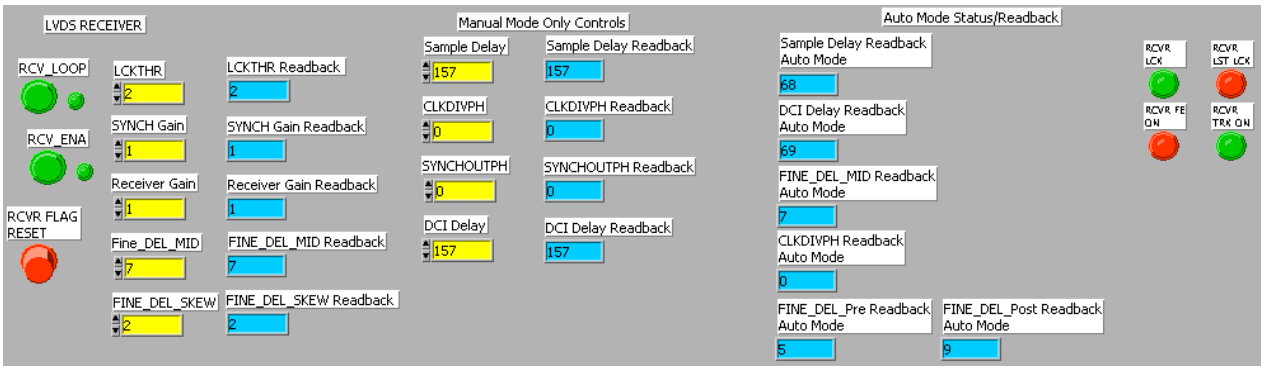

Figure 6

Another way to verify that the controller is in the correct spot (and not on the edge) is to check the status of the four status bits which sample the rising edge of the DCI at four different phases. *DCI PHS1* should always be high, and *DCI PHS3* should always be low. The other bits will toggle as the LVDS controller searches for the correct timing. The ideal case is shown in Figure 10. Increasing the value of the *FINE_DEL_SKEW* allows for a wider search around the DCI edge, and should reduce the toggling on *PHS0* and *PHS2*. This is usually required when the DCI signal has a lot of jitter.

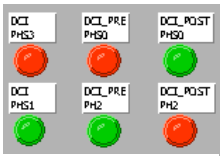

Figure 7

Result

The final result of this setup should be as shown in Figure 8. Note the RF Attenuation of 20dB to accurately measure harmonics.

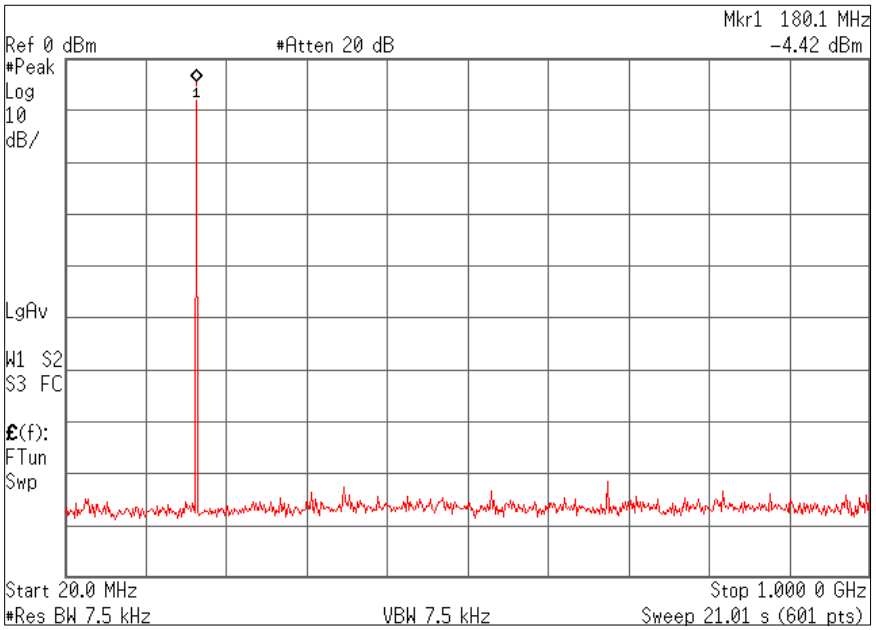

Figure 8

SPI SOFTWARE

The SPI software is broken up into numerous sections. Several of them are described here, as they pertain to the evaluation board. For complete descriptions of each SPI register, see the AD9737A/AD9739A datasheet. In the interest of continuous quality improvements, the images below may not exactly match your version of the software.

SPI Settings and Powerdown/Reset

These bits (shown in Figure 12) control the operation of the SPI port on the AD9737A/AD9739A, as well as the master reset and individual power-down bits. Changing the *SDIO DIR* or *DATADIR* bits will cause the SPI application to stop functioning correctly. Do not change these bits. The Reset button is "sticky", that is, the part will stay in reset for as long as the button is enabled. To reset the part, set this bit, run the SPI application, then unset this bit and run the application again.

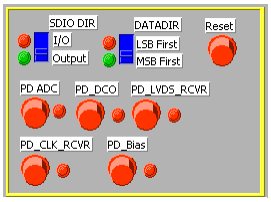

Figure 9

Controller Clock Controls and Analog FS controls

The Controller Clock controls enable the Mu Controller and LVDS controllers. For normal operation, both of these should be enabled. The *Clock GEN PD* switch powers down the clocking structure, and should be left disabled for normal use.

The DAC current ouput has an adjustable full-scale value. The *FSC Set* option allows for this adjustment. After running the SPI application, the full-scale current in miliamps will be displayed here.

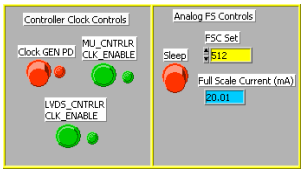

Figure 10

Mu Controller Clock Enable: Register 0x02 Bit 0
LVDS Controller Clock Enable: Register 0x02 Bit 1
Analog Full-Scale Setting (10 bit Gain DAC 10-30mA adjustment): Register 0x06 bit 0:8, Register 0x07 bits 0,1

Decoder Controller and IRQ Controls

Decoder Mode: Register 0x08 Bits 0,1

0x0 – Normal Mode
0x1 – Return to zero (RZ) Mode
0x2 – Mix Mode

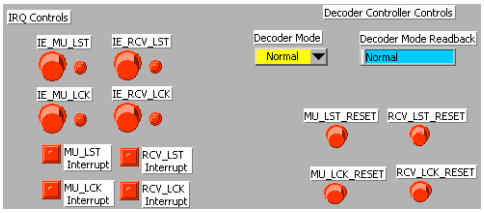

Figure 11

Cross Control

CLKP Offset Setting: Register 0x24 Bits 0-3
CLKP Direction Bit: Register 0x24 Bit 4
CLKP Offset Setting: Register 0x25 Bits 0-3
CLKP Direction Bit: Register 0x25 Bit 4
Damp: Register 0x25 Bits 7

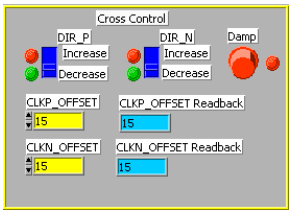

Figure 12

Mu Controller

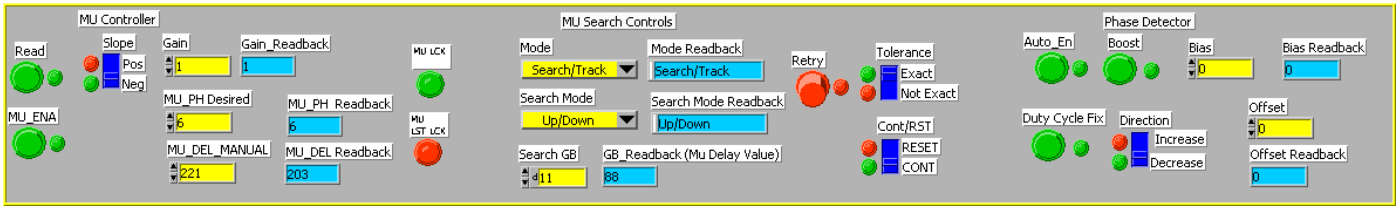

Figure 13

Mu Controller Enable: Register 0x26 Bit 0 (Set to 1 to enable the controller)

Mu Controller Gain: Register 0x26 Bits 1,2 (Optimal Setting is a Gain of 1)

MU Desired Phase: Desired Phase Value for Phase to Voltage Converter to Optimize Mu Controller. The optimal setting is negative 6 (max of 16) . Register 0x27 bits 0-4

Slope: Slope the mu contoller will lock onto Register 0x26 bit 6 (Optimal setting is Negative slope set bit to 0)

MU_DEL_Manual: Register 0x28 bits 0-7 and 0x27 bits 6,7: Sets the point where the Mu Controller begins to search. It is best to set it to the middle of the delay line . The maximum Mu delay is 432, so set these bits to approximately 220.

Mode: Register: 0x26 Bits 4, 5 Sets the Mode in which the Controller searches:

0x00 – Search and Track (Optimal Setting)

0x01 – Track Only

0x10 – Search Only

0x11 – Invalid

Search Mode: 0x27 – Bits 5, 6 Sets the Mode in which the search for the optimal phase is performed

0x00 – Down

0x01 – Up

0x10 – Up/Down (Optimal Setting)

0x11 – Invalid

Search GB: sets a GB from the beginning and end of the Mu Delay line in which the Mu controller will not enter into unless it does not find a valid phase outside the GB. Register 0x29 bits 0-4. Optimal value is Decimal 11.

Tolerance: Sets the Tolerance of the phase search. Register 0x29 bit 7

0 – Not Exact. Can find a phase within 2 phases of the desired phase

1- Exact. Finds the exact phase you are targeting (Optimal Setting)

ContRST: Controls whether the controller will reset or continue if it does not find the desired phase

0 – Continue (Optimal Setting)

1 – Reset

Phase Detector Enable: Register 0x24 bit 5. Enables the Phase Detector (Set to 1 to enable the Phase Detector)

Phase Detector Comparator Boost: Optimizes the bias to the Phase Detector (Set to 1 to enable)

Bias: Register 0x24 Bits 0-3: Manual Control of the bias if the Boost control is not enabled

Duty Cycle Fix: Register 0x25 Bit 7 Enables the duty cycle correction in the Mu Controller. Recommended to always enable (Set to 1 to enable)

Direction: Register 0x25 Bit 6 Sets the direction that the duty cycle will be corrected

0 – Negative (Optimal Setting)

1 - Positive

Offset: Register Register 0x25 Bit 0-5 Sets the Duty Cycle Correction manually if Fix is not enabled

The status read back bits for the mu controller are as follows:

MU_LCK: Register 0x2A bit 0 (value of 1 means the controller is locked)

LST_LCK: Register 0x2A bit 1 (Value of 1 means the control lost lock)

In order to read back the present MU Delay and phase value, it is necessary to set the Read bit high and then low before the values can be read back:

Read: Register 0x26 Bit 3

Mu Delay Readback: Register 0x28 bits 0-7 and 0x27 bits 6,7

(Total of 9 bits in the read back the maximum Mu delay value is d432 or x1B0)

MUD_PH_Readback: Register 0x27 bits 0-4 – Phase the controller locked to.

In order to use the Mu controller in manual mode the following bits are utilized:

Mu Controller Enable: Register 0x26 Bit 0 (Set to 0 to disable the controller)

MU_DEL_Manual: Register 0x28 bits 0-7 and 0x27 bits 7,8. (Total of 9 bits the maximum Mu delay value is d432 or x1B0)

LVDS Receiver Controls

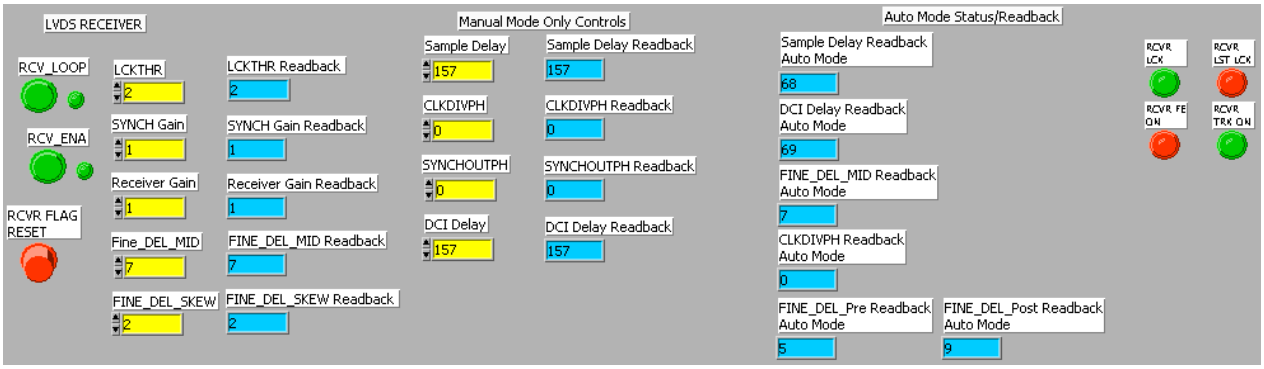

Figure 14

RCV_LOOP - On (Register 0x10 bit 1 set to 1)

RCV_ENA - On (Register 0x10 bit 0 set to 1)

LCKTHR - 2 (Register 0x15 bits 0-4)

RVCR_GAIN - 1 (Register 0x11 bit 0 set to 1)

FINE_DELAY_MID - 7 (Register 0x11 bits 2-5)

FINE_DELAY_SKEW - 2 (Register 0x13 bits 0-4)

Sample_Delay: Sets the midpoint where the controller begins to search Register 0x11 bits 6,7 Register 0x12 Optimal value is 166 which is the center of the delay line. The maximum delay value is d333 or x14D.

DCI_Delay: Must be equal to the Sample_delay. Register 0x13 bits 4-7 Register 0x14 bits 0-5. Optimal value is also 166 which is the center of the delay line. The maximum delay value is d333 or x14D.

To ensure that the LVDS Controller is locked and tracking check the status of the following bits:

RCVR Lock (Register 0x21 bit 0) This should be high if the controller is locked

TRK_ON (Register 0x21 bit 3) This should be high if the controller is tracking